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Development of a 3-phase, 4-wire, DSP controlled Power Quality Logger

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1. General approach to ADCs

1.1 Block diagram of four ADCs connected to the DSP managed by the microcontroller

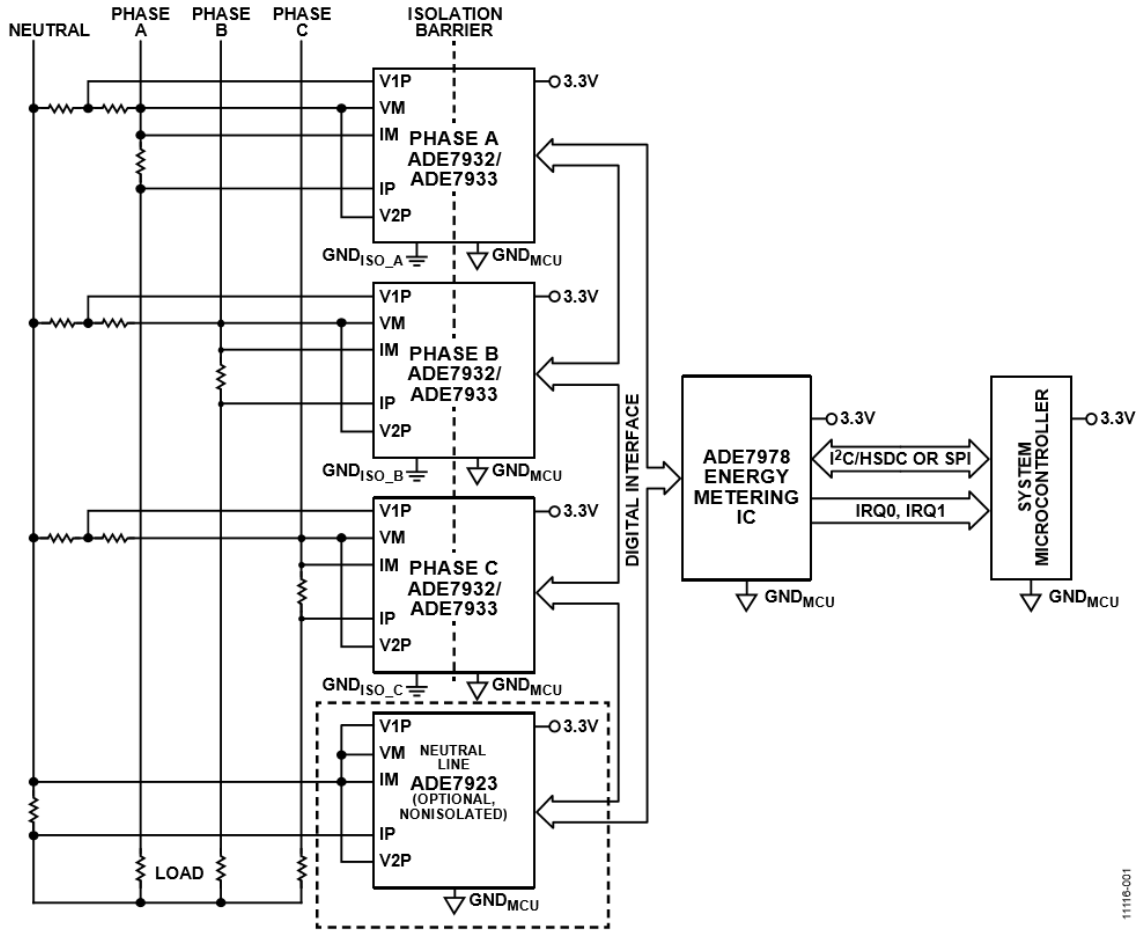


Figure 1: 3-phase, 4-Wire Meter with three ADE7933 devices and one ADE7978 DSP

1.2 ADC functional blockdiagram

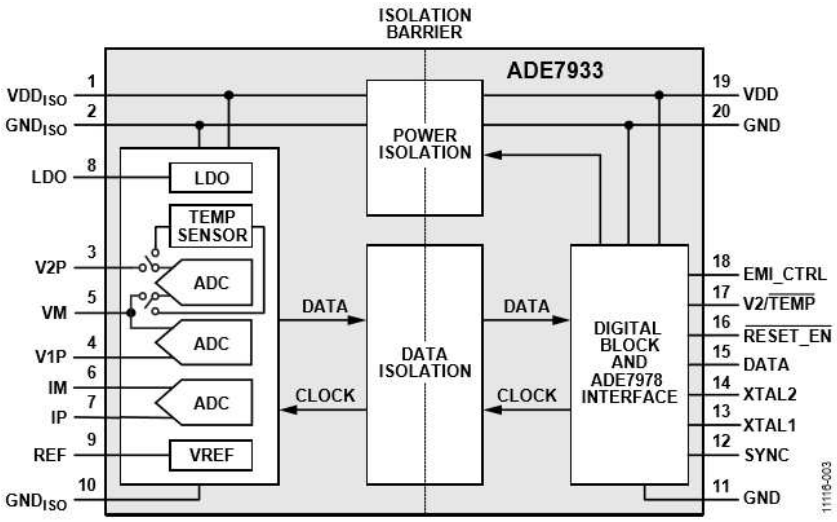


Figure 2: ADE7933 Functional Block Diagram

1.3 ADE7913 Overview : Isolated 3-Channel Sigma-Delta ADC with SPI

- 3 channel 24-bit ADC (simultaneously sampling with 3 ADE7913 ADC's possible)
- Up to 4 devices clocked on external clock
- Current channel = ±31,25mV nom. peak input range (± 5.320.000)
- Current channel = ±49,27mV max. peak input range (23bit = -8.388.608 tot +8.388.607)
- Voltage channel = ±500mV nom. peak input range (± 5.320.000)
- Voltage channel = ±788mV max. peak input range (23bit = -8.388.608 tot +8.388.607)
- **Voltage channel = 0,991 V/mV = 0,000991 V/µV = 0.000000991 V/nV**
- **Current channel = 0,5 A/mV = 0.0005 A/µV = 0.0000005 A/nV**
- Limit violation = digital LPF overflows which results in added harmonics due to the saturated code from this LPF output.
- **Internal reference = 1,2V**
- Single PS = 3,3V
- 20-SOIC
- -40°C to +85°C
- 24-bit signed 2's complement words
- 24 bits words generated @ **8ksps**
- XTAL in = 16.384Mhz
- Samplerate (oversampling) = CLKIN/16 = 16,384Mhz / 16 = **1024Mhz**
- Noise shaping + anti-aliasing

$MAX\ LSB_{voltage\ channel} = \frac{Full\ scale\ range(v)}{2^N(bits)} = \frac{788 \times 10^{-3}}{2^{23}} = 93{,}93692017\ nV/bit$
$NOM\ LSB_{current\ channel} = \frac{Full\ scale\ range(v)}{2^N(bits)} = \frac{500 \times 10^{-3}}{5.320.000} = 93{,}98496241 nV/bit$
$MAX\ LSB_{voltage\ channel} = \frac{Full\ scale\ range(v)}{2^N(bits)} = \frac{49{,}27 \times 10^{-3}}{2^{23}} = 5.873441696\ nV/bit$
$NOM\ LSB_{current\ channel} = \frac{Full\ scale\ range(v)}{2^N(bits)} = \frac{31.25 \times 10^{-3}}{5.320.000} = 5.874060150 nV/bit$

BITS	24
UNSIGNED MAX	16777215
UNSIGNED MIN	0
SIGNED MAX	8388607
SIGNED MIN	-8388608

1.4 Voltage channel: ADC transfert characteristics

ADC TRANSFER FUNCTION

	ADC TRANSFERT FUNCTION OF VOLTAGE CHANNEL							
	Peak input range (mV_{peak})	Peak grid voltage (V_{peak})	RMS grid Voltage (V)	Peak grid voltage/peak inputvoltage	ADC (Signed Int.)	ADC (Hex)	ADC (32-bit Hex)	Typical voltage channel ADC Offset Error (mV)
					8388607	0x 7FFFFF	0x 7F FFFF	
max	788	780,908	552,185	991	8384320			
nominal	500	495,5	350,371	991	5320000			
	250	247,75	175,186	991	10640000			
0	0	0	0,000	991	0	0	0	-35
	-250	-247,75	-175,186	991	-2660000			
nominal	-500	-495,5	-350,371	991	-5320000			
min	-788	-780,908	-552,185	991	-8384320			
					-8388608	0x 800000	0x FFFF FFFF FF80 0000	

1.5 Current channel: ADC transfert characteristics

	ADC TRANSFERT FUNCTION OF CURRENT CHANNEL							
	Peak input range (mV_{peak})	Peak grid current (A_{peak})	RMS grid current (A)	Peak grid current/peak input voltage range	ADC (Signed Int.)	Verschil	ADC (Hex)	
	49,28				8388607		0x 7F FFFF	
max	**49,27**	24,635	17,420	500	8387725	882		
nominal	**31,25**	15,625	11,049	500	5320000	3067725		
	10,00	5	3,536	500	1702400	3617600		
0	0,00	0	0,000	500	0	1702400	0	-2
	-10,00	-5	-3,536	500	-1702400	1702400		
nominal	**-31,25**	-15,625	-11,049	500	-5320000	3617600		
min	**-49,27**	-24,635	-17,420	500	-8387725	3067725		
	-49,28				-8388608	883	0x FFFF FFFF FF80 0000	

1.6 Design Targets

Range = 20A
Δi = 2mA
Rshunt = 2mΩ

1.7 Actual specification of ADE7933 with Rshunt = 2mΩ

- ✓ Ugrid-peak with guaranteed specification = 495,5V
- ✓ Ugrid-peak (ADC limit) = 780,908V
- ✓ Igrid-peak with guaranteed specification = 16A
- ✓ Igrid-peak (ADC limit) = 24,635A
- ✓ Hardware maximum current = 30A

1.8 Three-Phase, Four-wire, Wye distribution system

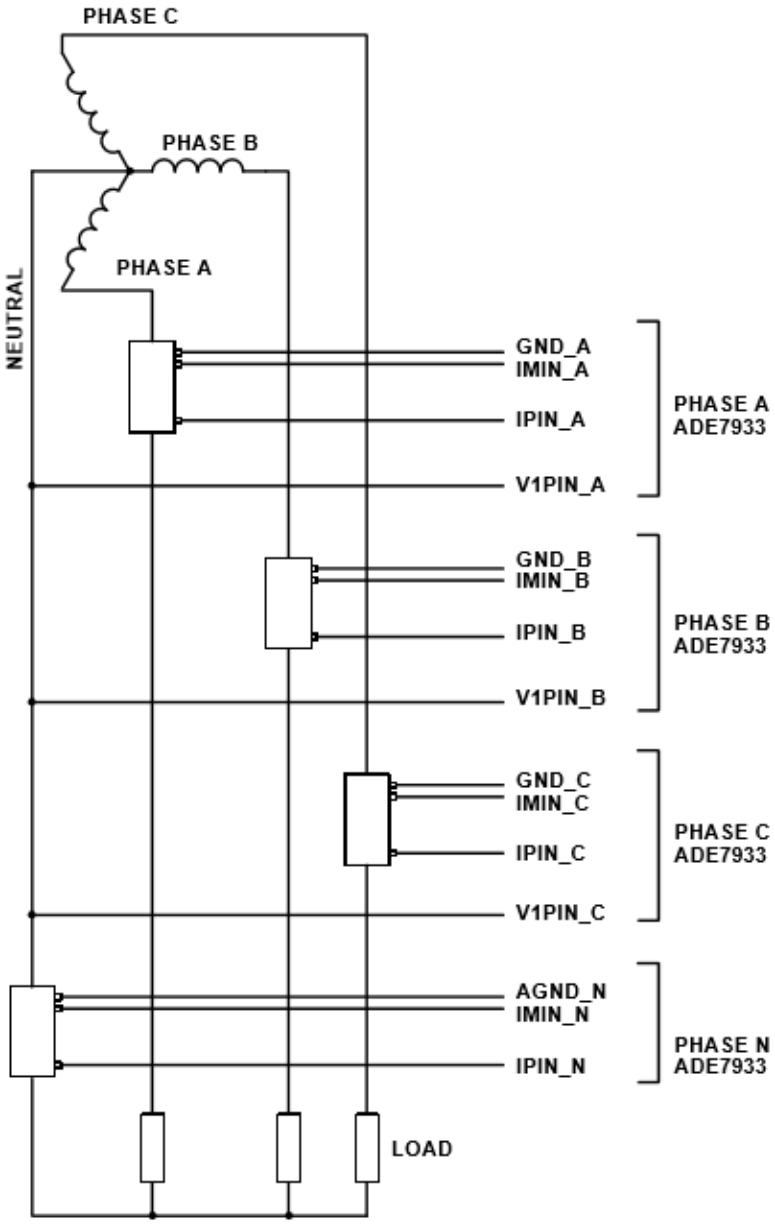


Figure 3: typical setup for ADE7978/ADE7933

2 General approach to the ADC resolution?

With this project we aim to move toward a higher resolution delta-sigma ADCs for voltage- and current sensing through shunt resistors. Besides a wide current range of 30A we want to be able to measure leakage flows with a high resolution. We aim at current measurements wit 5mA steps of resolution with a reasonable precision. A lot will depend on the total amount of noise in the system. All analog to digital conversions introduce a certain amount of noise into an electronic system. A number of factors are inherent to any ADC. For example, quantization noise is generated by the ADC conversion from analog to discrete steps because of the difference between the analog input signal and the discrete representation at the output of the ADC . We also have to be careful not to exceed the ADC limits because then noise is introduced due to the saturation of the ADC (=satuartion noise). Also and always present is the thermal noise (=Johnson noise) wich is generated by the thermal agitation of the charge carriers inside every electrical conductor. Thermal noise is present in every electrical ciruit, indepenant of any applied voltage. We also have to consider the external noise sources injected from radiating and/or conducting sources outside the electronic measurement system, espeecially the ADC input has tob e designed with care. The latter can be reduced to a minimum by correct design of the PCB and power source according to the EMC guidelines for PCB design.

Parameters such as effective resolution, noise-free resolution, ENOB, SINAD, SNR specifically describe how accurate an ADC exactly is. The other kinds of noise are not considered for now. SNR, SINAD and ENOB measure the ADC's dynamic performance.

2.1 The effective resolution

The effective resolution and noise-free resolution measure the ADC's noise performance at DC. So spectral distortion is not factored. (THD, SFDR)

$$\text{effective resolution} = \log_2\left[\frac{\text{full} - \text{scale input voltage range}}{\text{ADC}_{\text{RMS}_{\text{noise}}}}\right]$$

$$\text{effective resolution} = \log_2\left[\frac{V_{in}}{V_{\text{RMS}_{\text{noise}}}}\right]$$

The effective resolution should not be confused with ENOB. The methodolgy for measuring ENOB uses an FFT analysis of a sine-wave input tot he ADC.

2.2 The noise-free resolution

$$\text{noise} - \text{free resolution} = \log_2\left[\frac{\text{full} - \text{scale input voltage range}}{\text{ADC}_{\text{PP}_{\text{noise}}}}\right]$$

$$\text{noise} - \text{free resolution} = \log_2\left[\frac{V_{in}}{V_{\text{PP}_{\text{noise}}}}\right]$$

2.3 ENOB

$$\text{ENOB} = \log_2\left[\frac{\text{full}-\text{scale input voltage range}}{\text{ADC}_{\text{RMS}_{\text{noise}}} \times \sqrt{12}}\right]$$

2.4 SINAD

$$\text{SINAD} = \left[\frac{\text{RMS input voltage}}{\text{RMS noise voltage}}\right]$$

2.5 RMS noise

$$\text{RMS noise} = \frac{1}{M}\left[\sum_{m=0}^{M-1} E_{AVM(FM)}{}^{2}\right]$$

$E_{AVM}(FM)$ = averaged magnitude spectral component at a given discrete frequency after DFT

3 Datasheet ADE7933

3.1 Noise and distortion specifications page 8 and 9

SPECIFICATIONS

SYSTEM SPECIFICATIONS, ADE7978 AND ADE7933/ADE7932/ADE7923

VDD = 3.3 V ± 10%, GND = DGND = 0 V, ADE7978 XTALIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP} = 25°C.

Table 1.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
ACTIVE ENERGY MEASUREMENT					
Measurement Error (per Phase)					
Total Active Energy		0.1		%	Over a dynamic range of 500 to 1, power factor (PF) = 1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PF = 1
Fundamental Active Energy		0.1		%	Over a dynamic range of 500 to 1, PF = 1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PF = 1
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms at 50 Hz/100 Hz, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
Output Frequency Variation		0.01		%	
Total Active Energy Measurement Bandwidth		3.3		kHz	
REACTIVE ENERGY MEASUREMENT					
Measurement Error (per Phase)					
Total Reactive Power		0.1		%	Over a dynamic range of 500 to 1, PF = 0, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PF = 0
Fundamental Reactive Power		0.1		%	Over a dynamic range of 500 to 1, PF = 0, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PF = 0
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms at 50 Hz/100 Hz, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
Output Frequency Variation		0.01		%	
Total Reactive Energy Measurement Bandwidth		3.3		kHz	
RMS MEASUREMENTS					
Measurement Bandwidth		3.3		kHz	I rms and V rms
Voltage (V) rms Measurement Error		0.1		%	Over a dynamic range of 500 to 1
Current (I) rms Measurement Error		0.25		%	Over a dynamic range of 500 to 1
Fundamental V rms Measurement Error		0.1		%	Over a dynamic range of 500 to 1
Fundamental I rms Measurement Error		0.25		%	Over a dynamic range of 500 to 1
WAVEFORM SAMPLING					Sampling CLKIN/2048 (16.384 MHz/2048 = 8 kSPS)
Current Channels					See the Waveform Sampling Mode section
Signal-to-Noise Ratio (SNR)		67		dB	
Signal-to-Noise-and-Distortion (SINAD) Ratio		67		dB	
Total Harmonic Distortion (THD)		−85		dB	
Spurious-Free Dynamic Range (SFDR)		88		dBFS	

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
Voltage Channels					
SNR		75		dB	
SINAD Ratio		74		dB	
THD		−81		dB	
SFDR		81		dBFS	
Bandwidth (−3 dB)		3.3		kHz	
TIME INTERVAL BETWEEN PHASE SIGNALS					
Measurement Error		0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
CF1, CF2, CF3 PULSE OUTPUTS					
Maximum Output Frequency		68.8		kHz	WTHR = VARTHR = VATHR = 3, CFxDEN = 1, full scale current and voltage, PF = 1, one phase only
Duty Cycle		50		%	CF1, CF2, or CF3 frequency > 6.25 Hz, CFxDEN is even and > 1
		(1 + 1/CFxDEN) × 50		%	CF1, CF2, or CF3 frequency > 6.25 Hz, CFxDEN is odd and > 1
Active Low Pulse Width		80		ms	CF1, CF2, or CF3 frequency < 6.25 Hz
CF Jitter		0.04		%	CF1, CF2, or CF3 frequency = 1 Hz, nominal phase currents larger than 10% of full scale

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for definitions of the parameters.

Figure 4: ADE7933 datasheet

4 Quantification principles

4.1 Practical approach to quantification of ADC devices

Generalized Test Setup for FFT Analysis of ADC Output
There are a number of ways to quantify the distortion and noise of an ADC. All of them are based on an **FFT analysis** using a generalized test setup:

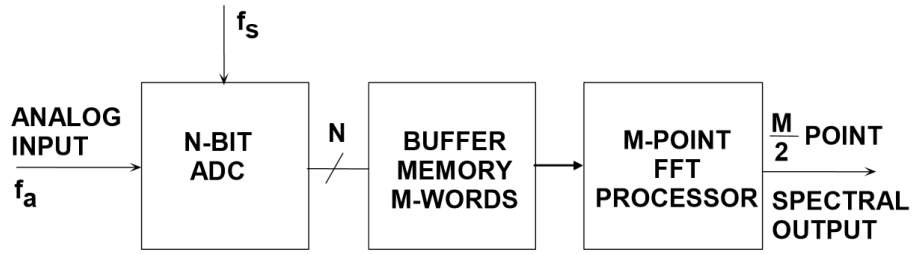


Figure 5:Generalized test setup for FFT analysis

4.2 Popular specifications for quantifying the ADC dynamic performance

SNR	signal-to-noise ratio
SINAD	signal-to-noise-and-distortion ratio
ENOB	effective number of bits
THD	total harmonic distortion
THD+N	total harmonic distortion + noise
SFDR	spurious free dynamic range

Most ADC manufacturers have adopted the same definitions for these specifications. They can be used for comparing different ADCs. It is important to:

- ✓ understand exactly **what** is being specified
- ✓ understand the **relationship between** these specifications

4.3 Parameters of sampling and FFT

Total frequency range covered is dc to $f_s/2$

- f_s = samplerate (Hz, samples/s, KSPS, MSPS)
- $f_s/2$ = Nyquist bandwidth
- Spectral output of FFT = series of M/2 points in the frequency domain
- M = Size of the FFT = number of samples stored in the buffer memory
- f_s/M = spacing between these M points = width of each frequency ”bin” = resolution of the FFT
- Theoretical noise floor = theoritical SNR + FFT process gain
- FFT process gain = 10xlog(M/2)

4.4 Important

The value for noise used in the SNR calculation is the noise that extends over the entire Nyquist bandwidth (dc to $f_s/2$), **but** the FFT acts as narrowband spectrum analyzer with a bandwidth of f_s/M that sweeps over the spectrum. This has the effect of pushing the noise down by an amount equal to the process gain. This is the same effect as narrowing the bandwidth of an analog spectrum analyzer.

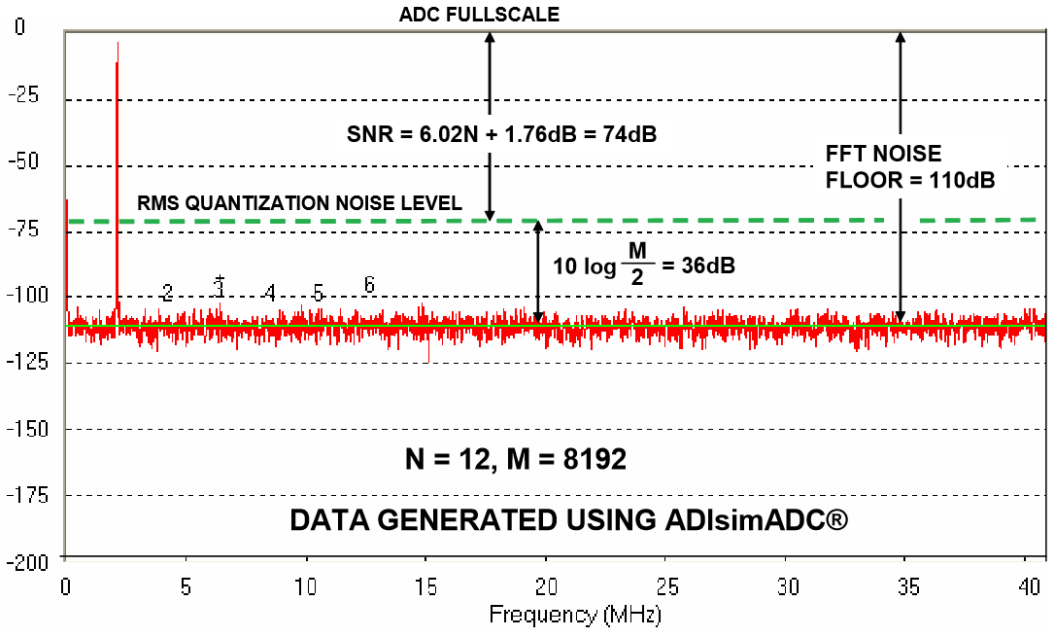


Figure 6: FFT Output for ideal 12-bit ADC, input = 2.111Mhz, fs = 82MSPS, Average of 5 FFTs, M=8192

4.5 FFT output

An FFT is can be compared to an **analog spectrum analyzer** that measures the amplitude of the harmonics and noise components of a digitized signal. The harmonics of the input signal can be distinguished from other distortion products by their location in the frequency spectrum. Here we see a 7MHz input signal sampled at 20 MSPS and the location of the first 9 harmonics.

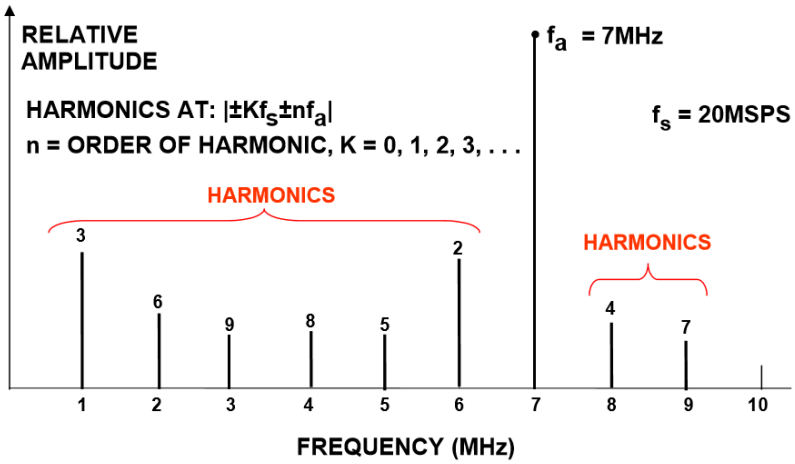
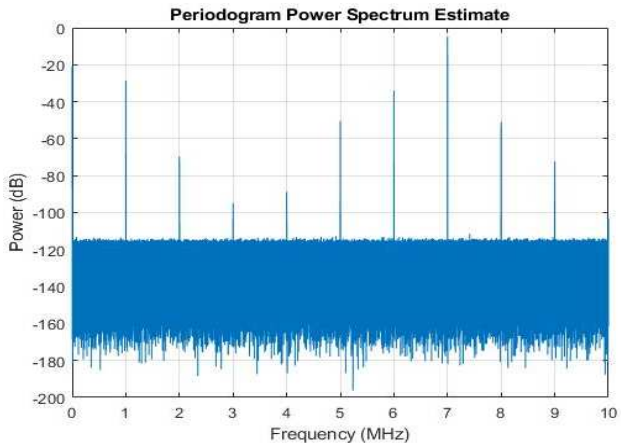


Figure 7 : Location of distortion products: Input Signal = 7MHz, Sampling rate = 20MSPS

<u>Aliased harmonics</u> of f_a fall at frequencies equal to $|\pm K.f_s \pm n.f_a|$
K = 0, 1, 2, 3, …
n = order of the harmonic (harmonic = multiple of base frequency)
The **2nd and 3rd harmonics** are generally the only ones specified on a data sheet because they tend to be the largest, altough some data sheets may specify the value of the **worst harmonic**.

4.6 Matlab example (without aliased harmonics)

```
>> Fs = 20000000;
f = 7000000;
t = 0:1/Fs:1;
x = tanh(sin(2*pi*f*t)+0.1) +
0.001*randn(1,length(t));
periodogram(x,kaiser(length(x),38),[],Fs,'power')
```



4.7 Total harmonic distortion (THD)

THD = the ratio of the mean value of the root-sum-square of its harmonics to the fundamental signal. Harmonic distortion is normally specified in **dBc** (decibels below carrier), altough in audio applications it may sometimes be specified as a **percentage**. Harmonic distortion is generally specified with an **input signal near full-scale** (generally 0.5 to 1 dB below full-scale to prevent clipping), but it can be specified at any level. For signals much lower than full-scale, other distortion products due to the differential nonlinearity (DNL) of the converter - not direct harmonics - may limit performance.
Only the lowest 5 harmonics are significant.

The THD can be calculated with n harmonics included

$$\mathrm{THD}_{dBc} = 20 \times \log\left(\frac{V^2_{2_{RMS}}+V^2_{3_{RMS}}+V^2_{4_{RMS}}+\cdots+V^2_{n_{RMS}}}{V^2_{1_{RMS}}}\right)$$ when n = 1 = fundamental frequency

$$\mathrm{THD}_{dBc} = 20 \times \log\left(\frac{\sqrt{V^2_{2_{RMS}} + V^2_{3_{RMS}} + V^2_{4_{RMS}} + \cdots + V^2_{n_{RMS}}}}{V_{1_{RMS}}}\right)$$

The THD can also be calculated with all harmonics included

$$\mathrm{THD}_{dBc} = 20 \times \log\left(\frac{V^2_{RMS} - V^2_1}{V^2_1}\right)$$

$$\mathrm{THD}_{dBc} = 20 \times \log\left(\frac{\sqrt{\sum_{n=2}^{\infty} V^2_{n\,RMS}}}{V_1}\right)$$

4.8 Total Harmonic Distortion + Noise (THD +N)

THD + N = the ratio of the mean value of the root-sum-square of its harmonics plus all noise components. (excluding dc) to the fundamental signal. The **BW** over which the noise is measured must be specified. In the case of an FFT, the bandwidth is **dc** to $\mathbf{f_s/2}$. If the BW of the measurement is dc to

$f_s/2$(=Nyquist BW), then **THD+N = SINAD** → Be warned, the measurement BW may not necessarily be the Nyquist BW.

4.9 Spurious free dynamic range (SFDR)

SFDR = the ratio of the **rms value of the signal** to the **rms value of the worst spurious signal** regardless of where it falls in the frequency spectrum. The worst spur may or may not be a harmonic of the original signal. SFDR is an important specification in communications systems because it represents the smallest value of signal that can be distinguished from a large interfering signal (blocker). SFDR can be specified with respect to full-scale (dBFS) or with respect to the actual signal amplitude (dBc). The definition of SFDR is shown graphically in Figure 4.

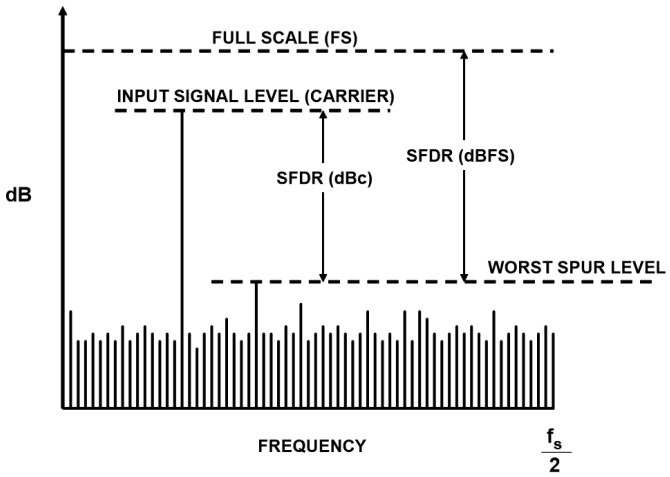


Figure 8: Spurious Free Dynamic Range (SFDR)

4.10 SINAD, SNR and ENOB

SINAD is a good overall dynamic performance of an ADC because it includes all components which make up noise and distortion. SINAD is often shown for different input amplitudes and frequencies. For a given frequency and amplitude, **SINAD** is equal to **THD + N**, provided the BW for the noise measurement is the same for both (=Nyquist BW)

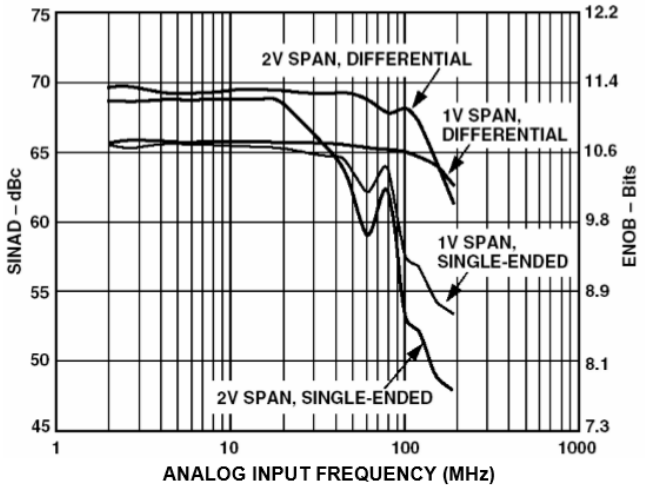


Figure 9: 12-bit, 65MSPS ADC SINAD and ENOB for various Input Full-Scale Spans (Range)

The figure shows that the ac performance of the ADC degrades due to high-frequency distortion and is usually plotted for frequencies well above the Nyquist frequency so that performance undersampling

applications can be evaluated. SINAD is often converted to ENOB (effective-number-of-bits) using the relationship for the **theoretical SNR** of an **ideal N-bit ADC**:

$$\text{SNR} = 6.02\text{N} + 1.76\text{dB}$$

The equation is solved for N, and the value of SINAD is substituted for SNR:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\text{dB}}{6.02}$$

(this equation assumes fullscale input signal)

Note that the last equation assumes a **full-scale input signal**. If the signal level is reduced, the value of SINAD decreases, and the ENOB decreases. It is necessary to add a correction factor for calculating ENOB at reduced signal amplitudes as shown in this formula :

$$\text{ENOB} = \frac{\text{SINAD}_{measured} - 1.76\text{dB} + 20\log\left(\frac{fullscale\ amplitude}{input\ amplitude}\right)}{6.02}$$

The correction factor essentially "normalizes" the ENOB value to full-scale regardless of the actual signal amplitude. Signal-to-noise ratio (SNR, or sometimes called SNR-without-harmonics) is calculated from the FFT data the same as SINAD, except that the signal harmonics are excluded from the calculation, leaving only the noise terms. In practice, it is only necessary to exclude the first 5 harmonics, since they dominate. The SNR plot will degrade at high input frequencies, but generally not as rapidly as SINAD because of the exclusion of the harmonic terms.

A few ADC data sheets somewhat loosely refer to SINAD as SNR, so you must be careful when interpreting these specifications and understand exactly what the manufacturer means.

4.11 Mathematical relationship between SINAD, SNR an THD

There is a mathematical relationship between SINAD, SNR, and THD (assuming all are measured with the same input signal amplitude and frequency. In the following equations, SNR, THD, and SINAD are expressed in dB, and are derived from the actual numerical ratios S/N, S/D, and S/(N+D) as shown below:

$$\text{SNR} = 20\log\left(\frac{S}{N}\right) \qquad THD = 20log\left(\frac{S}{D}\right) \qquad SINAD = 20log\left(\frac{S}{N+D}\right)$$

$$\frac{\text{N}}{\text{S}} = 10^{\frac{-\text{SNR}}{20}} \qquad \frac{\text{D}}{\text{S}} = 10^{\frac{-\text{THD}}{20}} \qquad \frac{\text{N+D}}{\text{S}} = 10^{\frac{-\text{SINAD}}{20}}$$

$$\frac{\text{N}+\text{D}}{\text{S}} = \left[\left(\frac{\text{N}}{\text{S}}\right)^2 + \left(\frac{\text{D}}{\text{S}}\right)^2\right]^{\frac{1}{2}} = \left[\left(10^{\frac{-SNR}{20}}\right)^2 + \left(10^{\frac{-THD}{20}}\right)^2\right]^{\frac{1}{2}} = \left[10^{\frac{-SNR}{10}} + 10^{\frac{-THD}{10}}\right]^{\frac{1}{2}}$$

$$\frac{\text{S}}{\text{N}+\text{D}} = \left[10^{\frac{-SNR}{10}} + 10^{\frac{-THD}{10}}\right]^{-\frac{1}{2}}$$

$$\text{SINAD} = 20\log\left(\frac{S}{N+D}\right) = -10log\left[10^{\frac{-SNR}{10}} + 10^{\frac{-THD}{10}}\right]$$ = SINAD as function of SNR and THD

$$\text{SNR} = 20\log\left(\frac{S}{N}\right) = -10log\left[10^{-\frac{SINAD}{10}} - 10^{-\frac{THD}{10}}\right]$$ = SNR from SINAD and THD

$$\text{THD} = 20\log\left(\frac{S}{D}\right) = -10log\left[10^{-\frac{SINAD}{10}} - 10^{-\frac{SNR}{10}}\right]$$ = THD from SINAD and SNR

It is important to emphasize that these relationships hold true only if the input frequency and amplitude are equal for all three measurements.

5 Quantification principles applied on the ADE7933

5.1 ADE7933 parameters for quantification of noise and distortion

Channels	Voltage	Current
BW(-3dB)	3,3kHz	3,3kHz
SNR	75dB	67dB
SINAD	74dB	67dB
THD	-81dB	-85dB
SFDR	81dBFS	88dBFS
ENOB Practical (@23-bits)	12 bits	10,84 bits

Figure 10: quantifying parameters

5.2 Calculation of ENOB

Effective number of bits is a parameter of the ADC's dynamic range. The number of bits used for storing a sampled analog point is the resolution. We can represent 2^N discrete signal levels with N-bits.

ENOB is based on the equation for an ideal ADC's SNR:

$$\text{SNR} = 6.02 \times \text{N} + 1.76 \text{ dB} \qquad (\text{N} = \text{ADC's resolution})$$

A real world ADC never achieves this SNR due to its own noise and errors. You can rearrange the equation to calculate an ADC's effective N, or ENOB as we commonly call it:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\text{dB}}{6.02}$$

5.3 Voltage channel ENOB distracted from specified parameters

$$\text{ENOB} = \frac{74\text{dB} - 1.76\text{dB}}{6.02} = 12\ bits$$

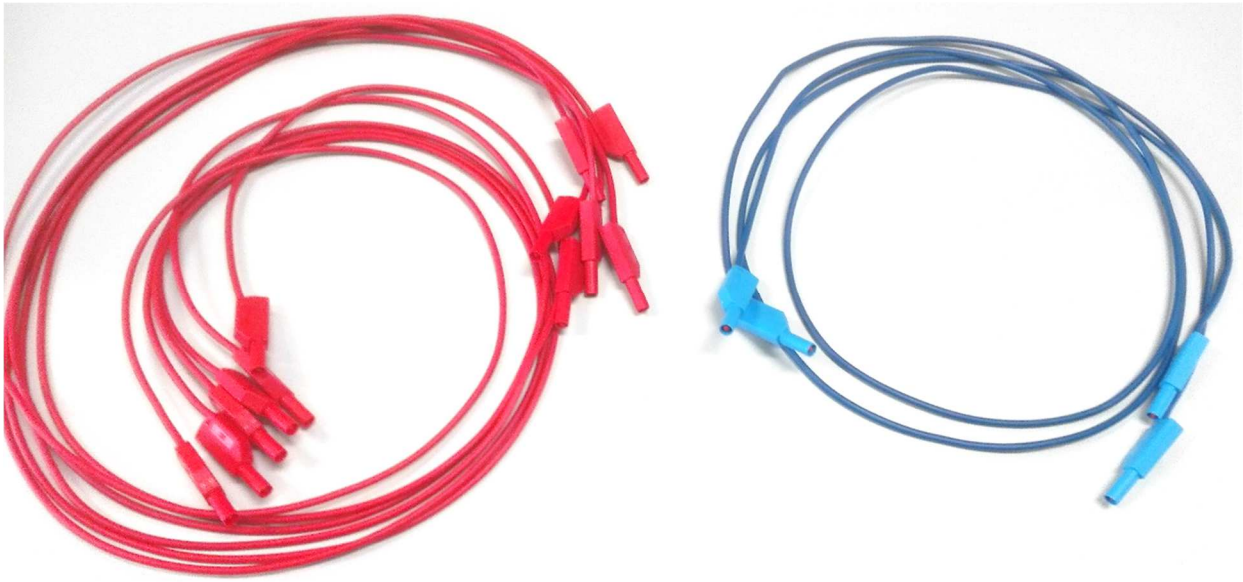
5.4 Current channel ENOB distracted from specified parameters

$$\text{ENOB} = \frac{67\text{dB} - 1.76\text{dB}}{6.02} = 10{,}84\ bits$$

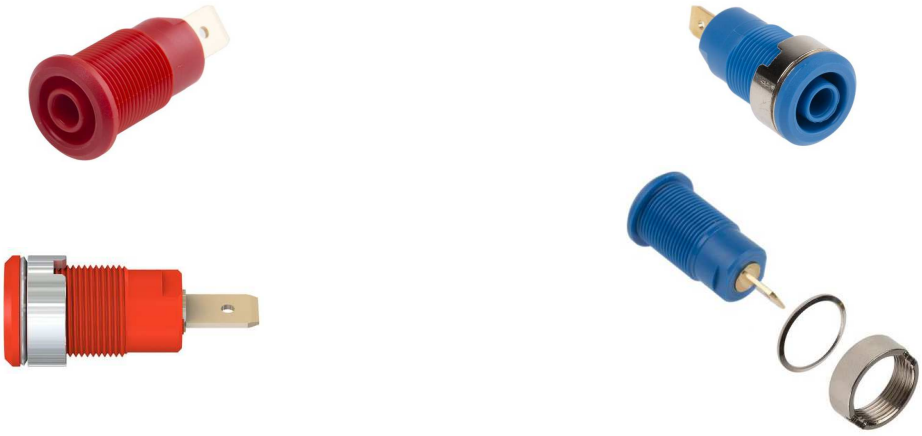
6 The hardware

6.1 AC power cord (link)

6.2 Eight 32A/1kV cables with secure male connector were constructed (cable surface = 4mm²)

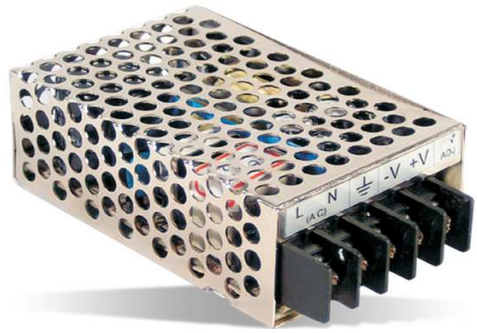


6.3 Eight 32A/1kV female connector mounted in a case (link)

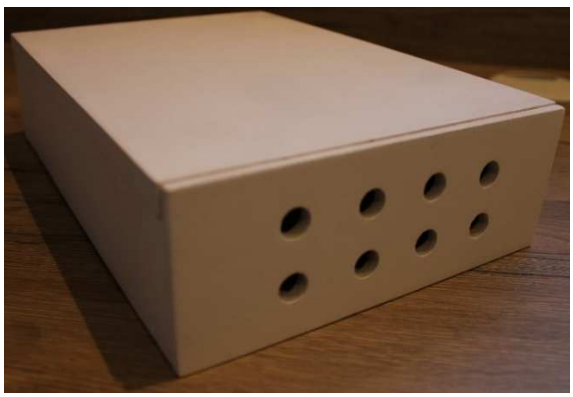


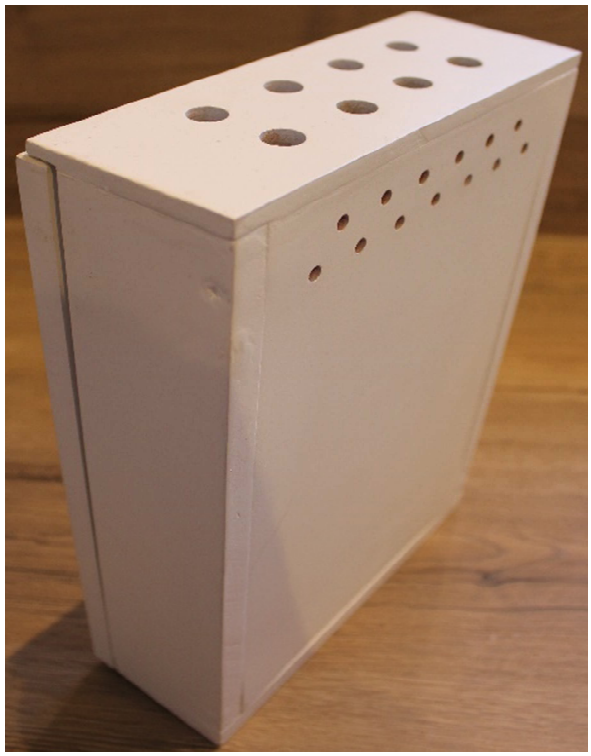
6.4 High Efficiency Switching Power supply RS25-12 – Mean Well (link)

Single output – 12V/25W/2.1A

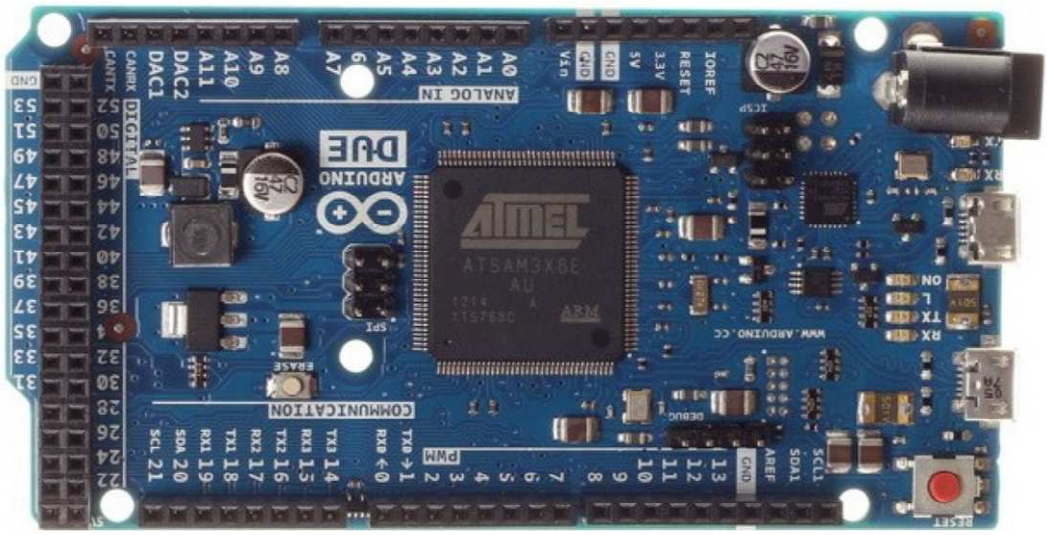


6.5 Painted case in fireproof material

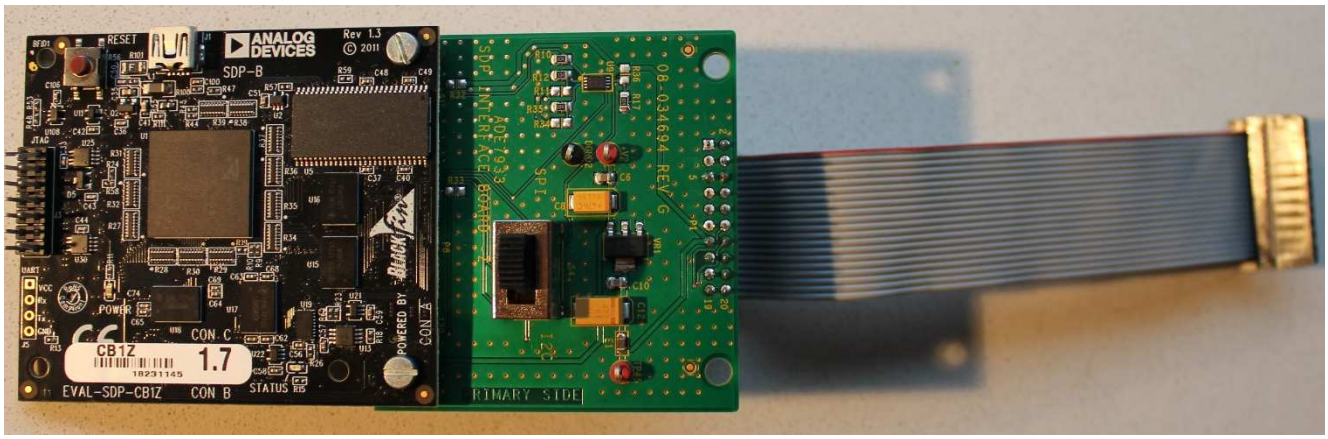




6.6 84Mhz Atmel SAM3X8E ARM Cortex-M3 CPU 32-bit ARM microcontroller



6.7 600Mhz ADSP-BF527: high performance 32-bit Blackfin embedded processor core



6.8 Shunt resistor set mounted on PCB design for >30A

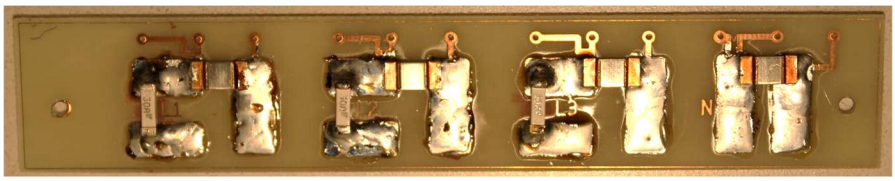
SMD 3921 0.002ohm 1% 4W Shunt Res AEC-Q200 75 PPM/C

6.9 30A – Fast fuses

250VAC 30A .00913ohms 463 NANO2

6.10 PCB with 4 shunt resistors of 2mΩ mounted on 2 x 75µm two sided FR4 material

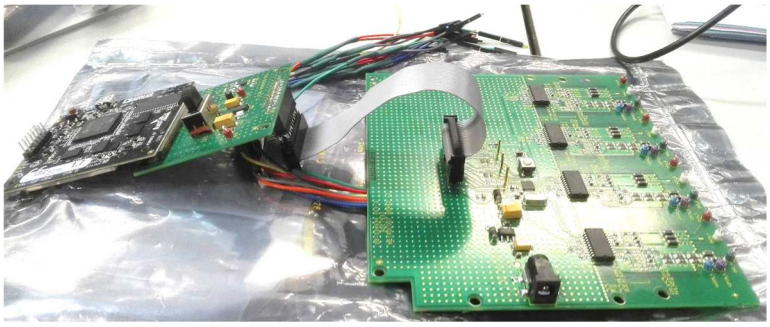
The devices pass Class B CISPR22/EN-55022 standard specification with a sufficient margin only with a 4-layer PCB.



6.11 3.0 CFM cooling fan for case cooling

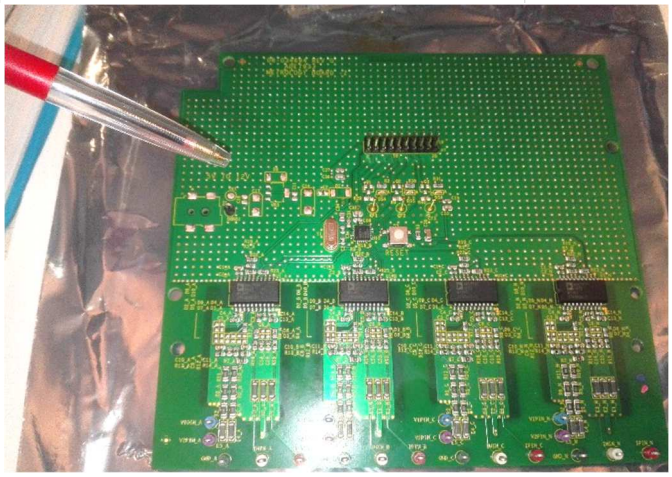
DC Fan, 25x10mm, 12VDC, **3CFM**, 0.36W, 16dBA, 9600RPM, 0.18inch H2O, Vapo Bearing, MagLev Motor. Rated current: 30 mA / max. 35 mA
Rated power consumption: 360mW / max. 420mW
Air flow: 3.0 CFM

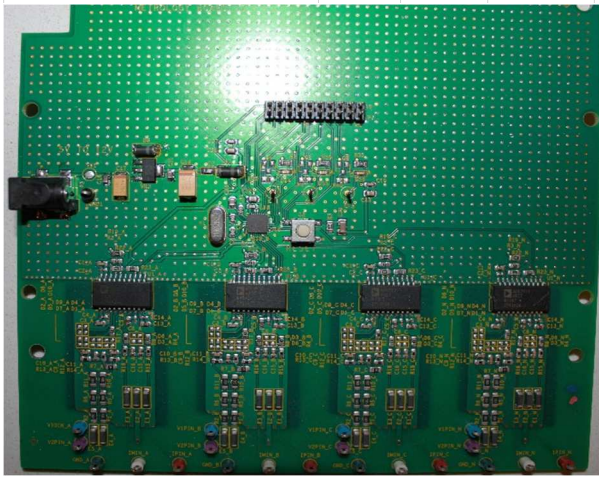
6.12 Flatcable for external configuration of the DSP



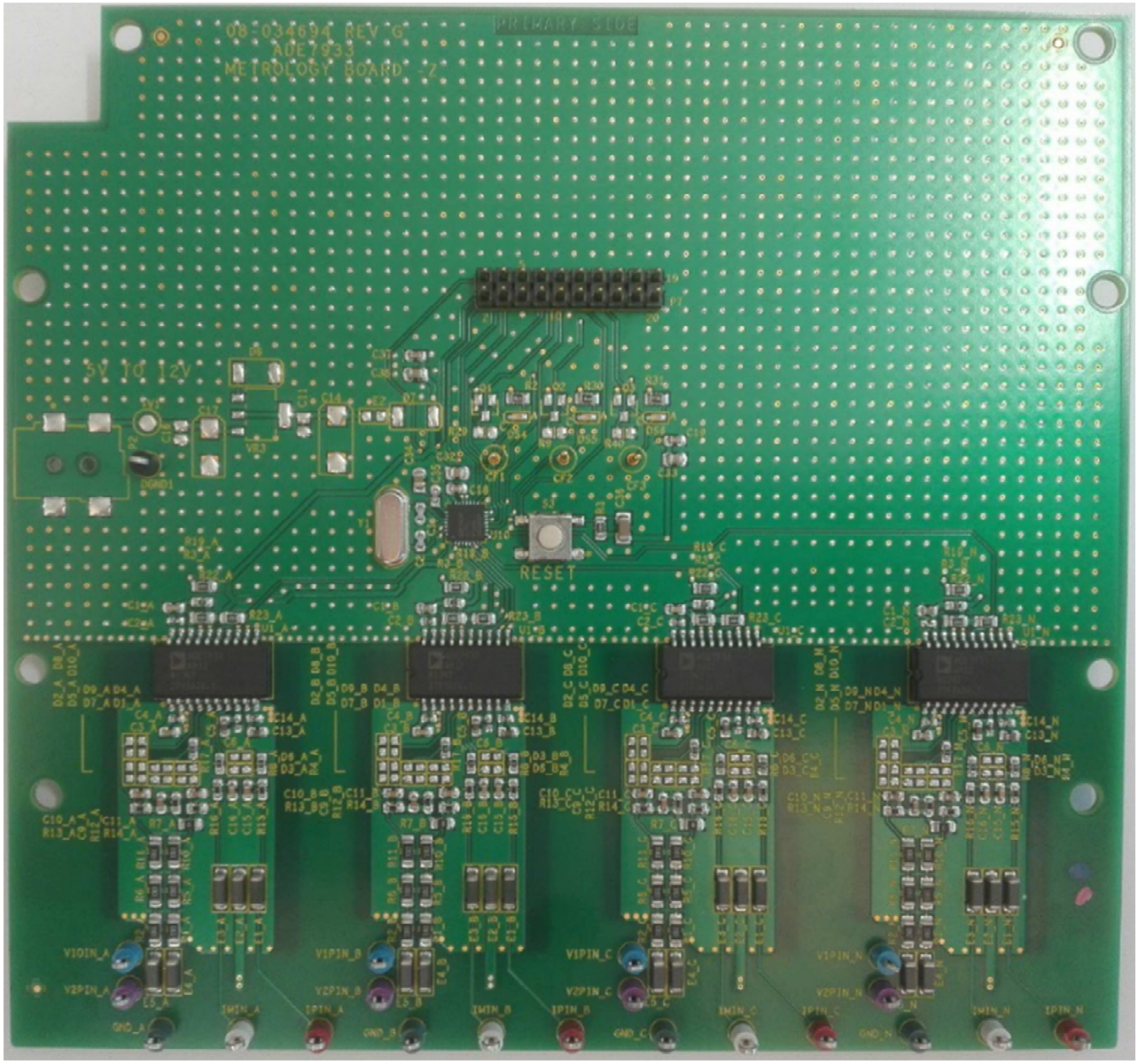
6.13 Extend PCB with additional SMD components for additional filtering and powering

DESCRIPTION	VALUE	JEDEC_TYPE	TOL	VOLTAGE	WATTAGE	LOCATION	MFG
Meerlaagse keramische condensatoren MLCC - SMD/SMT 0.1uF 50Volts X8R	0.1uF	C0805H53	10	50V		C11,C16	MURATA
Tantaalcondensatoren - vast SMD 6.3V 470uF 2917 10% ESR=100mOhms	470UF	C7343	10	6.3V		C14	KEMET
CAP TANT, WWPN: E000711	47uF	C6032	10	16	0	C17	AVX
DIODE RECT, WWPN: E001141	DL4001	DL41	N/A	50V		D6,D7	MICROSEMI
CONN-PCB 2MM CENTER PIN, RA, DC POWER JACK, WWPN: E000820	PJ-002AH-SMT	CNCUI-PJ-002A	NA	-0	-0	P2	CUI INC
800mA LOW-DROPOUT LINEAR REGULATOR, WWPN: E007641	LM1117MP-3.3/NOPB	SOT223		3.3V		VR3	NATIONAL
Ferrietparels HI CUR CHIP BD 0805 120OHMS 25% (100Mhz)	120OHM	0805 (2012 metric)	25	2,5A/120OHM			TAIYO YUDEN

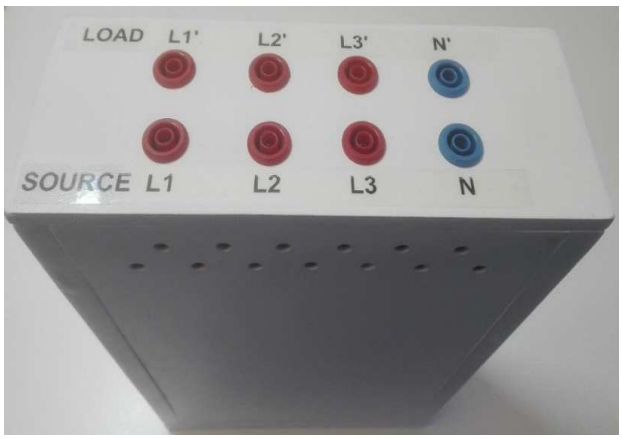




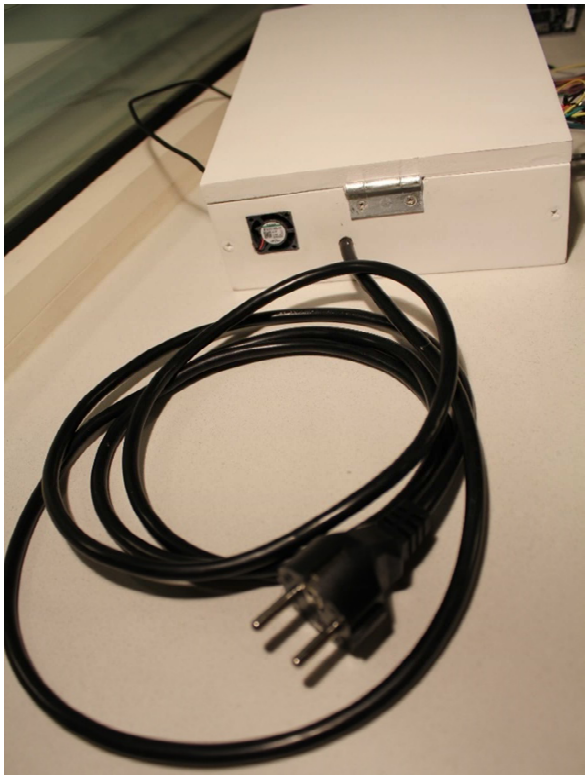
6.14 Printed Circuit Board: 3 x ADE7933 + 1x ADE7978



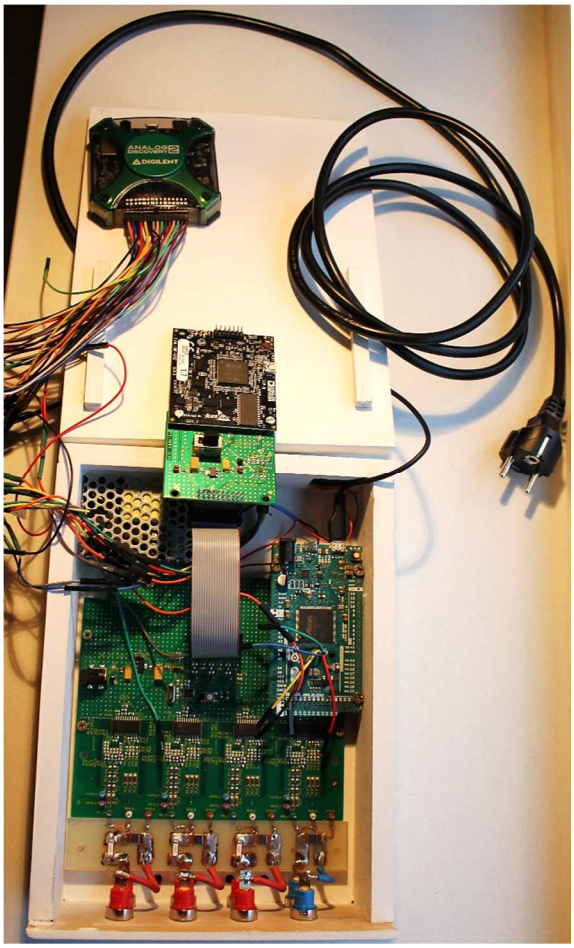
6.15 Front panel

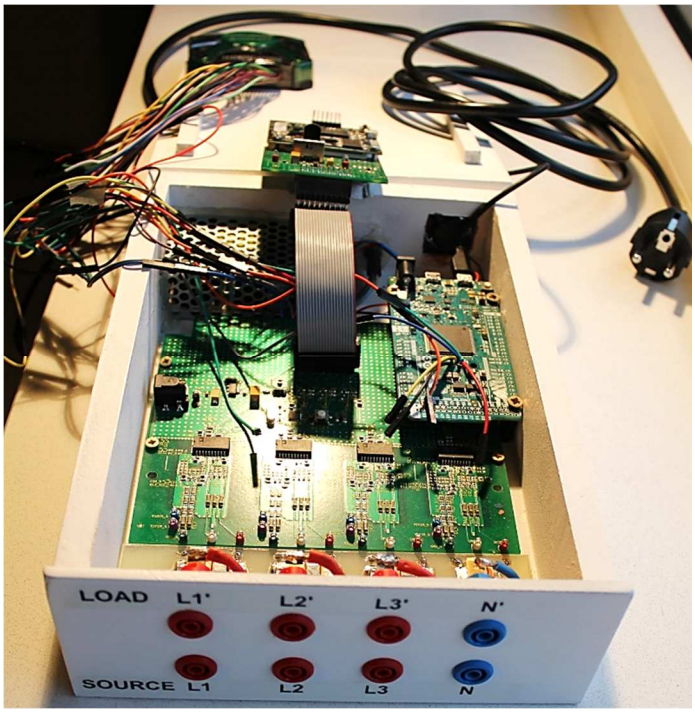


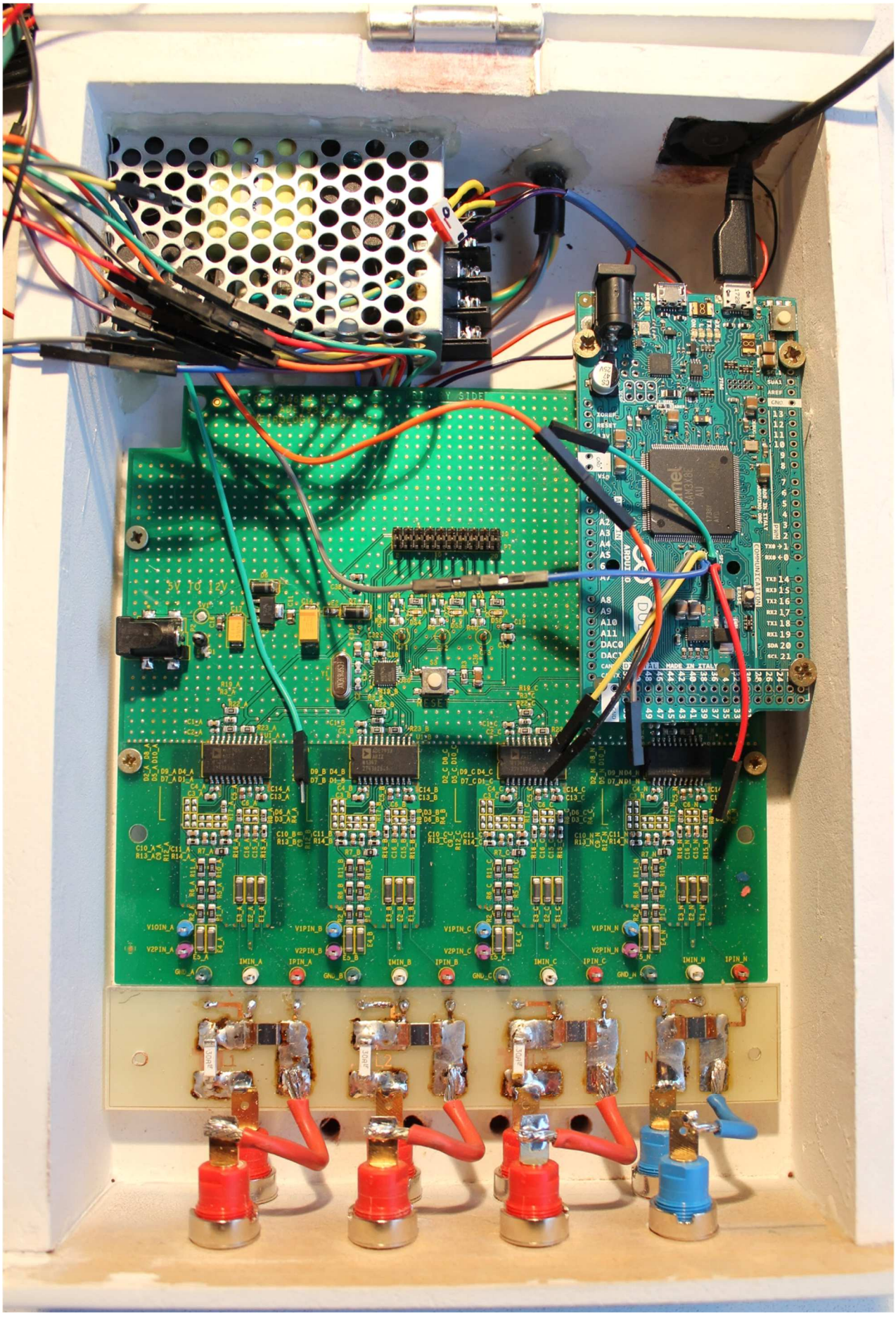
6.16 Backpanel



6.17 PCB mounted in case







7 The software

7.1 1973 Registers

The ADE7978 Digital Signal Processor contains **1973 registers** related to functionality, configuration and power quality measurements. Depending on its function, a register can be **read only**, **write only** or a combination of **read/write**. The word length of the DSP RAM registers consist of 32 bits, but the relevant data can vary from 8, 16, 24 to 32 bits depending its function. Some registers contain signed data and others contain unsigned data. Some values are formatted as twos complement numbers. It is important to take this into account when interacting with the registers.

7.2 General classification of the registers

- 128 registers are allocated to the DSP Data Memory RAM
- 38 registers are allocated to the Internal DSP Memory RAM
- 15 registers are assigned as Billable Registers
- 1792 registers are used as Configuration and Power Quality Registers

7.3 Register Terminology

R = read only
R / W = read and write
N / A = not applicable

32 ZPSE = 24-bit signed register that is transmitted as a 32-bit word with four MSBs padded with 0s and sign extended to 28 bits.

32 ZP = 28- or 24-bit signed or unsigned register that is transmitted as a 32-bit word with four MSBs or eight MSBs, respectively padded with 0s.

S = signed register in twos complement format
SE = sign extended to 28-bits

7.4 Register overview

7.4.1 Registers located in DSP Data Memory RAM (#128)

Table 39. Registers Located in DSP Data Memory RAM

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x4380	AIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A current gain adjust.
0x4381	AVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A voltage gain adjust.
0x4382	AV2GAIN	R/W	24	32 ZPSE	S	0x000000	Phase A V2P channel gain adjust.
0x4383	BIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B current gain adjust.
0x4384	BVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B voltage gain adjust.
0x4385	BV2GAIN	R/W	24	32 ZPSE	S	0x000000	Phase B V2P channel gain adjust.
0x4386	CIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C current gain adjust.
0x4387	CVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C voltage gain adjust.
0x4388	CV2GAIN	R/W	24	32 ZPSE	S	0x000000	Phase C V2P channel gain adjust.
0x4389	NIGAIN	R/W	24	32 ZPSE	S	0x000000	Neutral current gain adjust.
0x438A	NVGAIN	R/W	24	32 ZPSE	S	0x000000	Neutral line V1P channel gain adjust.
0x438B	NV2GAIN	R/W	24	32 ZPSE	S	0x000000	Neutral line V2P channel gain adjust.
0x438C	AIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A current rms offset.
0x438D	AVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A voltage rms offset.
0x438E	AV2RMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A V2P voltage rms offset.
0x438F	BIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B current rms offset.
0x4390	BVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B voltage rms offset.
0x4391	BV2RMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B V2P voltage rms offset.
0x4392	CIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C current rms offset.
0x4393	CVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C voltage rms offset.
0x4394	CV2RMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C V2P voltage rms offset.
0x4395	NIRMSOS	R/W	24	32 ZPSE	S	0x000000	Neutral current rms offset.
0x4396	NVRMSOS	R/W	24	32 ZPSE	S	0x000000	Neutral line V1P voltage rms offset.
0x4397	NV2RMSOS	R/W	24	32 ZPSE	S	0x000000	Neutral line V2P voltage rms offset.
0x4398	ISUMLVL	R/W	24	32 ZPSE	S	0x000000	Threshold used to compare the absolute sum of phase currents and the neutral current.
0x4399	APGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A power gain adjust.
0x439A	BPGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B power gain adjust.
0x439B	CPGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C power gain adjust.
0x439C	AWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A total active power offset adjust.
0x439D	BWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B total active power offset adjust.
0x439E	CWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C total active power offset adjust.
0x439F	AVAROS	R/W	24	32 ZPSE	S	0x000000	Phase A total reactive power offset adjust.
0x43A0	BVAROS	R/W	24	32 ZPSE	S	0x000000	Phase B total reactive power offset adjust.
0x43A1	CVAROS	R/W	24	32 ZPSE	S	0x000000	Phase C total reactive power offset adjust.
0x43A2	VLEVEL	R/W	24	32 ZPSE	S	0x000000	Register used in the algorithm that computes the fundamental active and reactive powers. See Equation 28.
0x43A3	AFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental active power offset adjust.
0x43A4	BFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental active power offset adjust.
0x43A5	CFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental active power offset adjust.
0x43A6	AFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental reactive power offset adjust.
0x43A7	BFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental reactive power offset adjust.
0x43A8	CFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental reactive power offset adjust.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x43A9	AFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental current rms offset.
0x43AA	BFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental current rms offset.
0x43AB	CFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental current rms offset.
0x43AC	AFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental voltage rms offset.
0x43AD	BFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental voltage rms offset.
0x43AE	CFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental voltage rms offset.
0x43AF	TEMPCO	R/W	24	32 ZPSE	S	0x000000	Temperature coefficient of the shunt.
0x43B0	ATEMP0	R/W	24	32 ZPSE	S	0x000000	Phase A ADE7933/ADE7932 ambient temperature at calibration.
0x43B1	BTEMP0	R/W	24	32 ZPSE	S	0x000000	Phase B ADE7933/ADE7932 ambient temperature at calibration.
0x43B2	CTEMP0	R/W	24	32 ZPSE	S	0x000000	Phase C ADE7933/ADE7932 ambient temperature at calibration.
0x43B3	NTEMP0	R/W	24	32 ZPSE	S	0x000000	Neutral line ADE7923 or ADE7933/ADE7932 ambient temperature at calibration.
0x43B4	ATGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A temperature gain adjust.
0x43B5	BTGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B temperature gain adjust.
0x43B6	CTGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C temperature gain adjust.
0x43B7	NTGAIN	R/W	24	32 ZPSE	S	0x000000	Neutral line temperature gain adjust.
0x43B8 to 0x43BF	Reserved	N/A	N/A	N/A	N/A	0x000000	These memory locations should be kept at 0x000000 for proper operation.
0x43C0	AIRMS	R	24	32 ZP	S	N/A	Phase A current rms value.
0x43C1	AVRMS	R	24	32 ZP	S	N/A	Phase A voltage rms value.
0x43C2	AV2RMS	R	24	32 ZP	S	N/A	Phase A V2P voltage rms value.
0x43C3	BIRMS	R	24	32 ZP	S	N/A	Phase B current rms value.
0x43C4	BVRMS	R	24	32 ZP	S	N/A	Phase B voltage rms value.
0x43C5	BV2RMS	R	24	32 ZP	S	N/A	Phase B V2P voltage rms value.
0x43C6	CIRMS	R	24	32 ZP	S	N/A	Phase C current rms value.
0x43C7	CVRMS	R	24	32 ZP	S	N/A	Phase C voltage rms value.
0x43C8	CV2RMS	R	24	32 ZP	S	N/A	Phase C V2P voltage rms value.
0x43C9	NIRMS	R	24	32 ZP	S	N/A	Neutral current rms value.
0x43CA	ISUM	R	28	32 ZP	S	N/A	Sum of IAWV, IBWV, and ICWV registers.
0x43CB	ATEMP	R	24	32 ZP	S	N/A	Phase A ADE7933/ADE7932 temperature.
0x43CC	BTEMP	R	24	32 ZP	S	N/A	Phase B ADE7933/ADE7932 temperature.
0x43CD	CTEMP	R	24	32 ZP	S	N/A	Phase C ADE7933/ADE7932 temperature.
0x43CE	NTEMP	R	24	32 ZP	S	N/A	Neutral line ADE7923 or ADE7933/ADE7932 temperature.
0x43CF to 0x43FF	Reserved	N/A	N/A	N/A	N/A	0x000000	These memory locations should be kept at 0x000000 for proper operation.

[1] R = read only; R/W = read and write; N/A = not applicable.
[2] 32 ZPSE = 24-bit signed register that is transmitted as a 32-bit word with four MSBs padded with 0s and sign extended to 28 bits. 32 ZP = 28- or 24-bit signed or unsigned register that is transmitted as a 32-bit word with four MSBs or eight MSBs, respectively, padded with 0s.
[3] S = signed register in twos complement format.

7.4.2 Internal DSP Memory RAM registers (#38)

Table 40. Internal DSP Memory RAM Registers

Address	Register Name	R/W[1]	Bit Length	Type[2]	Default Value	Description
0xE203	Reserved	R/W	16	U	0x0000	This address should not be written for proper operation.
0xE228	Run	R/W	16	U	0x0000	The run register starts and stops the DSP (see the Digital Signal Processor section).

[1] R/W = read and write.
[2] U = unsigned register.

7.4.3 Billable Registers (#15)

Table 41. Billable Registers

Address	Register Name	R/W[1]	Bit Length	Type[2]	Default Value	Description
0xE400	AWATTHR	R	32	S	0x00000000	Phase A total active energy accumulation.
0xE401	BWATTHR	R	32	S	0x00000000	Phase B total active energy accumulation.
0xE402	CWATTHR	R	32	S	0x00000000	Phase C total active energy accumulation.
0xE403	AFWATTHR	R	32	S	0x00000000	Phase A fundamental active energy accumulation.
0xE404	BFWATTHR	R	32	S	0x00000000	Phase B fundamental active energy accumulation.
0xE405	CFWATTHR	R	32	S	0x00000000	Phase C fundamental active energy accumulation.
0xE406	AVARHR	R	32	S	0x00000000	Phase A total reactive energy accumulation.
0xE407	BVARHR	R	32	S	0x00000000	Phase B total reactive energy accumulation.
0xE408	CVARHR	R	32	S	0x00000000	Phase C total reactive energy accumulation.
0xE409	AFVARHR	R	32	S	0x00000000	Phase A fundamental reactive energy accumulation.
0xE40A	BFVARHR	R	32	S	0x00000000	Phase B fundamental reactive energy accumulation.
0xE40B	CFVARHR	R	32	S	0x00000000	Phase C fundamental reactive energy accumulation.
0xE40C	AVAHR	R	32	S	0x00000000	Phase A apparent energy accumulation.
0xE40D	BVAHR	R	32	S	0x00000000	Phase B apparent energy accumulation.
0xE40E	CVAHR	R	32	S	0x00000000	Phase C apparent energy accumulation.

[1] R = read only.
[2] S = signed register in twos complement format.

7.4.4 Configuration an Power Quality Registers (#1792 – Address range: 0xE500 to 0xEBFF)

Table 42. Configuration and Power Quality Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE500	IPEAK	R	32	32	U	N/A	Current peak register (see Figure 70 and Table 43 for more information).
0xE501	VPEAK	R	32	32	U	N/A	Voltage peak register (see Figure 70 and Table 44 for more information).
0xE502	STATUS0	R/W	32	32	U	N/A	Interrupt Status Register 0 (see Table 45).
0xE503	STATUS1	R/W	32	32	U	N/A	Interrupt Status Register 1 (see Table 46).
0xE504 to 0xE506	Reserved						These addresses should not be written for proper operation.
0xE507	OILVL	R/W	24	32 ZP	U	0xFFFFFF	Overcurrent threshold.
0xE508	OVLVL	R/W	24	32 ZP	U	0xFFFFFF	Overvoltage threshold.
0xE509	SAGLVL	R/W	24	32 ZP	U	0x000000	Voltage sag level threshold.
0xE50A	MASK0	R/W	32	32	U	0x00000000	Interrupt Enable Register 0 (see Table 47).
0xE50B	MASK1	R/W	32	32	U	0x00000000	Interrupt Enable Register 1 (see Table 48).
0xE50C	IAWV	R	24	32 SE	S	N/A	Instantaneous value of Phase A current.
0xE50D	IBWV	R	24	32 SE	S	N/A	Instantaneous value of Phase B current.
0xE50E	ICWV	R	24	32 SE	S	N/A	Instantaneous value of Phase C current.
0xE50F	INWV	R	24	32 SE	S	N/A	Instantaneous value of neutral current.
0xE510	VAWV	R	24	32 SE	S	N/A	Instantaneous value of Phase A voltage.
0xE511	VBWV	R	24	32 SE	S	N/A	Instantaneous value of Phase B voltage.
0xE512	VCWV	R	24	32 SE	S	N/A	Instantaneous value of Phase C voltage.
0xE513	VA2WV	R	24	32 SE	S	N/A	Instantaneous value of Phase A V2P voltage.
0xE514	VB2WV	R	24	32 SE	S	N/A	Instantaneous value of Phase B V2P voltage.
0xE515	VC2WV	R	24	32 SE	S	N/A	Instantaneous value of Phase C V2P voltage.
0xE516	VNWV	R	24	32 SE	S	N/A	Instantaneous value of neutral line V1P voltage.
0xE517	VN2WV	R	24	32 SE	S	N/A	Instantaneous value of neutral line V2P voltage.
0xE518	AWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase A total active power.
0xE519	BWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase B total active power.
0xE51A	CWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase C total active power.
0xE51B	AVAR	R	24	32 SE	S	N/A	Instantaneous value of Phase A total reactive power.
0xE51C	BVAR	R	24	32 SE	S	N/A	Instantaneous value of Phase B total reactive power.
0xE51D	CVAR	R	24	32 SE	S	N/A	Instantaneous value of Phase C total reactive power.
0xE51E	AVA	R	24	32 SE	S	N/A	Instantaneous value of Phase A apparent power.
0xE51F	BVA	R	24	32 SE	S	N/A	Instantaneous value of Phase B apparent power.
0xE520	CVA	R	24	32 SE	S	N/A	Instantaneous value of Phase C apparent power.
0xE521	AVTHD	R	24	32 ZP	S	N/A	Total harmonic distortion of Phase A voltage.
0xE522	AITHD	R	24	32 ZP	S	N/A	Total harmonic distortion of Phase A current.
0xE523	BVTHD	R	24	32 ZP	S	N/A	Total harmonic distortion of Phase B voltage.
0xE524	BITHD	R	24	32 ZP	S	N/A	Total harmonic distortion of Phase B current.
0xE525	CVTHD	R	24	32 ZP	S	N/A	Total harmonic distortion of Phase C voltage.
0xE526	CITHD	R	24	32 ZP	S	N/A	Total harmonic distortion of Phase C current.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE527 to 0xE52F	Reserved						These addresses should not be written for proper operation.
0xE530	NVRMS	R	24	32 ZP	S	N/A	Neutral line V1P voltage rms value.
0xE531	NV2RMS	R	24	32 ZP	S	N/A	Neutral line V2P voltage rms value.
0xE532	CHECKSUM	R	32	32	U	0x6BF87803	Checksum verification (see the Checksum Register section for more information).
0xE533	VNOM	R/W	24	32 ZP	S	0x000000	Nominal phase voltage rms used in the alternative computation of the apparent power.
0xE534 to 0xE536	Reserved						These addresses should not be written for proper operation.
0xE537	AFIRMS	R	24	32 ZP	S	N/A	Phase A fundamental current rms value.
0xE538	AFVRMS	R	24	32 ZP	S	N/A	Phase A fundamental voltage rms value.
0xE539	BFIRMS	R	24	32 ZP	S	N/A	Phase B fundamental current rms value.
0xE53A	BFVRMS	R	24	32 ZP	S	N/A	Phase B fundamental voltage rms value.
0xE53B	CFIRMS	R	24	32 ZP	S	N/A	Phase C fundamental current rms value.
0xE53C	CFVRMS	R	24	32 ZP	S	N/A	Phase C fundamental voltage rms value.
0xE53D to 0xE5FE	Reserved						These addresses should not be written for proper operation.
0xE5FF	LAST_ RWDATA32	R	32	32	U	N/A	Contains the data from the last successful 32-bit register communication.
0xE600	PHSTATUS	R	16	16	U	N/A	Phase peak register (see Table 49).
0xE601	ANGLE0	R	16	16	U	N/A	Time Delay 0 (see the Time Interval Between Phases section for more information).
0xE602	ANGLE1	R	16	16	U	N/A	Time Delay 1 (see the Time Interval Between Phases section for more information).
0xE603	ANGLE2	R	16	16	U	N/A	Time Delay 2 (see the Time Interval Between Phases section for more information).
0xE604 to 0xE607	Reserved						These addresses should not be written for proper operation.
0xE608	PHNOLOAD	R	16	16	U	N/A	Phase no load register (see Table 50).
0xE609 to 0xE60B	Reserved						These addresses should not be written for proper operation.
0xE60C	LINECYC	R/W	16	16	U	0xFFFF	Line cycle accumulation mode count.
0xE60D	ZXTOUT	R/W	16	16	U	0xFFFF	Zero-crossing timeout count.
0xE60E	COMPMODE	R/W	16	16	U	0x01FF	Computation mode register (see Table 51).
0xE60F	Reserved						This address should not be written for proper operation.
0xE610	CFMODE	R/W	16	16	U	0x0E88	CFx configuration register (see Table 52).
0xE611	CF1DEN	R/W	16	16	U	0x0000	CF1 denominator.
0xE612	CF2DEN	R/W	16	16	U	0x0000	CF2 denominator.
0xE613	CF3DEN	R/W	16	16	U	0x0000	CF3 denominator.
0xE614	APHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of Phase A (see Table 53).
0xE615	BPHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of Phase B (see Table 53).
0xE616	CPHCAL	R/W	10	16 ZP	U	0x0000	Phase calibration of Phase C (see Table 53).
0xE617	PHSIGN	R	16	16	U	N/A	Power sign register (see Table 54).
0xE618	CONFIG	R/W	16	16	U	0x0010	ADE7978 configuration register (see Table 55).
0xE619 to 0xE6FF	Reserved						These addresses should not be written for proper operation.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE700	MMODE	R/W	8	8	U	0x1C	Measurement mode register (see Table 56).
0xE701	ACCMODE	R/W	8	8	U	0x80	Accumulation mode register (see Table 57).
0xE702	LCYCMODE	R/W	8	8	U	0x78	Line accumulation mode behavior (see Table 59).
0xE703	PEAKCYC	R/W	8	8	U	0x00	Peak detection half line cycles.
0xE704	SAGCYC	R/W	8	8	U	0x00	Sag detection half line cycles.
0xE705	CFCYC	R/W	8	8	U	0x01	Number of CF pulses between two consecutive energy latches (see the Synchronizing Energy Registers with the CFx Outputs section).
0xE706	HSDC_CFG	R/W	8	8	U	0x00	HSDC configuration register (see Table 60).
0xE707	Version	R	8	8	U		Version of die.
0xE708	CONFIG3	R/W	8	8	U	0x0F	ADE7933/ADE7932 or ADE7923 configuration register (see Table 61).
0xE709	ATEMPOS	R	8	8	S	N/A	Phase A ADE7933/ADE7932 temperature sensor offset (see the Second Voltage Channel and Temperature Measurement section)
0xE70A	BTEMPOS	R	8	8	S	N/A	Phase B ADE7933/ADE7932 temperature sensor offset (see Second Voltage Channel and Temperature Measurement section)
0xE70B	CTEMPOS	R	8	8	S	N/A	Phase C ADE7933/ADE7932 temperature sensor offset (see Second Voltage Channel and Temperature Measurement section
0xE70C	NTEMPOS	R	8	8	S	N/A	Neutral line ADE7923 or ADE7933/ADE7932 temperature sensor offset (see Second Voltage Channel and Temperature Measurement section)
0xE70D to 0xE7E2	Reserved						These addresses should not be written for proper operation.
0xE7E3	Reserved	R/W	8	8	U	N/A	Internal register used in conjunction with the internal register at Address 0xE7FE to enable/disable the protection of the DSP RAM-based registers (see the Digital Signal Processor section for more information).
0xE7E4 to 0xE7FC	Reserved						These addresses should not be written for proper operation.
0xE7FD	LAST_ RWDATA8	R	8	8	U	N/A	Contains the data from the last successful 8-bit register communication.
0xE7FE	Reserved	R/W	8	8	U	N/A	Internal register used in conjunction with the internal register at Address 0xE7E3 to enable/disable the protection of the DSP RAM-based registers (see the Digital Signal Processor section for more information).
0xE7FF to 0xE901	Reserved						These addresses should not be written for proper operation.
0xE902	APF	R	16	16	U	N/A	Phase A power factor.
0xE903	BPF	R	16	16	U	N/A	Phase B power factor.
0xE904	CPF	R	16	16	U	N/A	Phase C power factor.
0xE905	APERIOD	R	16	16	U	N/A	Line period on Phase A voltage.
0xE906	BPERIOD	R	16	16	U	N/A	Line period on Phase B voltage.
0xE907	CPERIOD	R	16	16	U	N/A	Line period on Phase C voltage.
0xE908	APNOLOAD	R/W	16	16	U	0x0000	No load threshold in the total/fundamental active power datapath.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE909	VARNOLOAD	R/W	16	16	U	0x0000	No load threshold in the total/fundamental reactive power datapath.
0xE90A	VANOLOAD	R/W	16	16	U	0x0000	No load threshold in the apparent power datapath.
0xE90B to 0xE9FD	Reserved						These addresses should not be written for proper operation.
0xE9FE	LAST_ADD	R	16	16	U	N/A	Contains the address of the register accessed during the last successful read or write operation.
0xE9FF	LAST_ RWDATA16	R	16	16	U	N/A	Contains the data from the last successful 16-bit register communication.
0xEA00	CONFIG2	R/W	8	8	U	0x00	Configuration register (see Table 62).
0xEA01	LAST_OP	R	8	8	U	N/A	Indicates the type (read or write) of the last successful read or write operation.
0xEA02	WTHR	R/W	8	8	U	0x03	Threshold used in phase total/fundamental active energy datapath.
0xEA03	VARTHR	R/W	8	8	U	0x03	Threshold used in phase total/fundamental reactive energy datapath.
0xEA04	VATHR	R/W	8	8	U	0x03	Threshold used in phase apparent energy datapath.
0xEA05 to 0xEBFE	Reserved		8	8			These addresses should not be written for proper operation.
0xEBFF	Reserved		8	8			This address can be used to manipulate the $\overline{SS}$/HSA pin when SPI is chosen as the active port. See the Serial Interfaces section for more information.

[1] R = read only; R/W = read and write.
[2] 32 ZP = 24-bit signed or unsigned register that is transmitted as a 32-bit word with eight MSBs padded with 0s. 32 SE = 24-bit signed register that is transmitted as a 32-bit word sign extended to 32 bits. 16 ZP = 10-bit unsigned register that is transmitted as a 16-bit word with six MSBs padded with 0s.
[3] U = unsigned register; S = signed register in twos complement format.
[4] N/A = not applicable.

7.4.5 IPEAK (Address 0xE500 – Length 32 bits)

Table 43. IPEAK Register (Address 0xE500)

Bits	Bit Name	Default Value	Description
[23:0]	IPEAKVAL[23:0]	0	These bits contain the peak value determined in the current channel.
24	IPPHASE[0]	0	When this bit is set to 1, the Phase A current generated the IPEAKVAL[23:0] value.
25	IPPHASE[1]	0	When this bit is set to 1, the Phase B current generated the IPEAKVAL[23:0] value.
26	IPPHASE[2]	0	When this bit is set to 1, the Phase C current generated the IPEAKVAL[23:0] value.
[31:27]		00000	These bits are always set to 0.

7.4.6 VPEAK (Address 0xE501 – Length 32 bits)

Table 44. VPEAK Register (Address 0xE501)

Bits	Bit Name	Default Value	Description
[23:0]	VPEAKVAL[23:0]	0	These bits contain the peak value determined in the voltage channel.
24	VPPHASE[0]	0	When this bit is set to 1, the Phase A voltage generated the VPEAKVAL[23:0] value.
25	VPPHASE[1]	0	When this bit is set to 1, the Phase B voltage generated the VPEAKVAL[23:0] value.
26	VPPHASE[2]	0	When this bit is set to 1, the Phase C voltage generated the VPEAKVAL[23:0] value.
[31:27]		00000	These bits are always set to 0.

7.4.7 STATUS0 Register (Address 0xE502 – Length 32 bits)

Table 45. STATUS0 Register (Address 0xE502)

Bits	Bit Name	Default Value	Description
0	AEHF	0	When this bit is set to 1, it indicates that Bit 30 in one of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR) has changed.
1	FAEHF	0	When this bit is set to 1, it indicates that Bit 30 in one of the fundamental active energy registers (FWATTHR, BFWATTHR, or CFWATTHR) has changed.
2	REHF	0	When this bit is set to 1, it indicates that Bit 30 in one of the total reactive energy registers (AVARHR, BVARHR, or CVARHR) has changed.
3	FREHF	0	When this bit is set to 1, it indicates that Bit 30 in one of the fundamental reactive energy registers (AFVARHR, BFVARHR, or CFVARHR) has changed.
4	VAEHF	0	When this bit is set to 1, it indicates that Bit 30 in one of the apparent energy registers (AVAHR, BVAHR, or CVAHR) has changed.
5	LENERGY	0	When this bit is set to 1, it indicates the end of an integration over the integer number of half line cycles set in the LINECYC register (line cycle energy accumulation mode).
6	REVAPA	0	When this bit is set to 1, it indicates that the Phase A active power (total or fundamental) identified by Bit 0 (REVAPSEL) in the MMODE register has changed sign. The sign itself is indicated in Bit 0 (AWSIGN) of the PHSIGN register (see Table 54).
7	REVAPB	0	When this bit is set to 1, it indicates that the Phase B active power (total or fundamental) identified by Bit 0 (REVAPSEL) in the MMODE register has changed sign. The sign itself is indicated in Bit 1 (BWSIGN) of the PHSIGN register (see Table 54).
8	REVAPC	0	When this bit is set to 1, it indicates that the Phase C active power (total or fundamental) identified by Bit 0 (REVAPSEL) in the MMODE register has changed sign. The sign itself is indicated in Bit 2 (CWSIGN) of the PHSIGN register (see Table 54).
9	REVPSUM1	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF1 datapath has changed sign. The sign itself is indicated in Bit 3 (SUM1SIGN) of the PHSIGN register (see Table 54).
10	REVRPA	0	When this bit is set to 1, it indicates that the Phase A reactive power (total or fundamental) identified by Bit 1 (REVRPSEL) in the MMODE register has changed sign. The sign itself is indicated in Bit 4 (AVARSIGN) of the PHSIGN register (see Table 54).
11	REVRPB	0	When this bit is set to 1, it indicates that the Phase B reactive power (total or fundamental) identified by Bit 1 (REVRPSEL) in the MMODE register has changed sign. The sign itself is indicated in Bit 5 (BVARSIGN) of the PHSIGN register (see Table 54).
12	REVRPC	0	When this bit is set to 1, it indicates that the Phase C reactive power (total or fundamental) identified by Bit 1 (REVRPSEL) in the MMODE register has changed sign. The sign itself is indicated in Bit 6 (CVARSIGN) of the PHSIGN register (see Table 54).
13	REVPSUM2	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF2 datapath has changed sign. The sign itself is indicated in Bit 7 (SUM2SIGN) of the PHSIGN register (see Table 54).
14	CF1	0	When this bit is set to 1, it indicates that a high to low transition has occurred at the CF1 pin; that is, an active low pulse has been generated. This bit is set even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL[2:0]) in the CFMODE register (see Table 52).
15	CF2	0	When this bit is set to 1, it indicates that a high to low transition has occurred at the CF2 pin; that is, an active low pulse has been generated. This bit is set even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bits[5:3] (CF2SEL[2:0]) in the CFMODE register (see Table 52).
16	CF3	0	When this bit is set to 1, it indicates that a high to low transition has occurred at the CF3 pin; that is, an active low pulse has been generated. This bit is set even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL[2:0]) in the CFMODE register (see Table 52).
17	DREADY	0	When this bit is set to 1, it indicates that all periodical (8 kHz rate) DSP computations have finished.
18	REVPSUM3	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF3 datapath has changed sign. The sign itself is indicated in Bit 8 (SUM3SIGN) of the PHSIGN register (see Table 54).
[31:19]	Reserved	0 0000 0000 0000	Reserved. These bits are always set to 0.

7.4.8 STATUS1 Register (Address 0xE503 – Length 32 bits)

Table 46. STATUS1 Register (Address 0xE503)

Bits	Bit Name	Default Value	Description
0	NLOAD	0	When this bit is set to 1, it indicates that at least one phase entered or exited the no load condition based on the total active and reactive powers. The phase is indicated in Bits[2:0] (NLPHASE[x]) in the PHNOLOAD register (see Table 50).
1	FNLOAD	0	When this bit is set to 1, it indicates that at least one phase entered or exited the no load condition based on the fundamental active and reactive powers. The phase is indicated in Bits[5:3] (FNLPHASE[x]) in the PHNOLOAD register (see Table 50).
2	VANLOAD	0	When this bit is set to 1, it indicates that at least one phase entered or exited the no load condition based on the apparent power. The phase is indicated in Bits[8:6] (VANLPHASE[x]) in the PHNOLOAD register (see Table 50).
3	ZXTOVA	0	When this bit is set to 1, it indicates that a zero crossing on the Phase A voltage is missing.
4	ZXTOVB	0	When this bit is set to 1, it indicates that a zero crossing on the Phase B voltage is missing.
5	ZXTOVC	0	When this bit is set to 1, it indicates that a zero crossing on the Phase C voltage is missing.
6	ZXTOIA	0	When this bit is set to 1, it indicates that a zero crossing on the Phase A current is missing.
7	ZXTOIB	0	When this bit is set to 1, it indicates that a zero crossing on the Phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it indicates that a zero crossing on the Phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it indicates that a zero crossing was detected on the Phase A voltage.
10	ZXVB	0	When this bit is set to 1, it indicates that a zero crossing was detected on the Phase B voltage.
11	ZXVC	0	When this bit is set to 1, it indicates that a zero crossing was detected on the Phase C voltage.
12	ZXIA	0	When this bit is set to 1, it indicates that a zero crossing was detected on the Phase A current.
13	ZXIB	0	When this bit is set to 1, it indicates that a zero crossing was detected on the Phase B current.
14	ZXIC	0	When this bit is set to 1, it indicates that a zero crossing was detected on the Phase C current.
15	RSTDONE	1	At the end of a hardware or software reset, this bit is set to 1, and the $\overline{IRQ1}$ pin goes low. To clear this interrupt and return the $\overline{IRQ1}$ pin high, write a 1 to this bit. The RSTDONE interrupt cannot be masked; therefore, this bit must always be reset to 0 for the $\overline{IRQ1}$ pin to return high.
16	Sag	0	When this bit is set to 1, it indicates that a sag event occurred on the phase indicated by Bits[14:12] (VSPHASE[x]) in the PHSTATUS register (see Table 49).
17	OI	0	When this bit is set to 1, it indicates that an overcurrent event occurred on the phase indicated by Bits[5:3] (OIPHASE[x]) in the PHSTATUS register (see Table 49).
18	OV	0	When this bit is set to 1, it indicates that an overvoltage event occurred on the phase indicated by Bits[11:9] (OVPHASE[x]) in the PHSTATUS register (see Table 49).
19	SEQERR	0	When this bit is set to 1, it indicates that a negative to positive zero crossing on the Phase A voltage was followed by a negative to positive zero crossing on the Phase C voltage instead of on the Phase B voltage.
20	MISMTCH	0	When this bit is set to 1, it indicates that ||ISUM| – |INWV|| > |ISUMLVL|, where ISUMLVL is the value of the ISUMLVL register (Address 0x4398). For more information, see the Neutral Current Mismatch section.
21	Reserved	1	Reserved. This bit is always set to 1.
22	Reserved	0	Reserved. This bit is always set to 0.
23	PKI	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the current channel has ended. The IPEAK register contains the peak value and the phase where the peak was detected (see Table 43).
24	PKV	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the voltage channel has ended. The VPEAK register contains the peak value and the phase where the peak was detected (see Table 44).
25	CRC	0	When this bit is set to 1, it indicates that the ADE7978 has computed a checksum value that is different from the checksum value computed when the run register was set to 1.
[31:26]	Reserved	00 0000	Reserved. These bits are always set to 0.

7.4.9 MASK0 Register (Address 0xE50A – Length 32 bits)

Table 47. MASK0 Register (Address 0xE50A)

Bits	Bit Name	Default Value	Description
0	AEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 changes in any of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR).
1	FAEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 changes in any of the fundamental active energy registers (AFWATTHR, BFWATTHR, or CFWATTHR).
2	REHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 changes in any of the total reactive energy registers (AVARHR, BVARHR, or CVARHR).
3	FREHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 changes in any of the fundamental reactive energy registers (AFVARHR, BFVARHR, or CFVARHR).
4	VAEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 changes in any of the apparent energy registers (AVAHR, BVAHR, or CVAHR).
5	LENERGY	0	When this bit is set to 1, it enables an interrupt at the end of an integration over the integer number of half line cycles set in the LINECYC register (line cycle energy accumulation mode).
6	REVAPA	0	When this bit is set to 1, it enables an interrupt when the Phase A active power (total or fundamental) identified by Bit 0 (REVAPSEL) in the MMODE register changes sign.
7	REVAPB	0	When this bit is set to 1, it enables an interrupt when the Phase B active power (total or fundamental) identified by Bit 0 (REVAPSEL) in the MMODE register changes sign.
8	REVAPC	0	When this bit is set to 1, it enables an interrupt when the Phase C active power (total or fundamental) identified by Bit 0 (REVAPSEL) in the MMODE register changes sign.
9	REVPSUM1	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF1 datapath changes sign.
10	REVRPA	0	When this bit is set to 1, it enables an interrupt when the Phase A reactive power (total or fundamental) identified by Bit 1 (REVRPSEL) in the MMODE register changes sign.
11	REVRPB	0	When this bit is set to 1, it enables an interrupt when the Phase B reactive power (total or fundamental) identified by Bit 1 (REVRPSEL) in the MMODE register changes sign.
12	REVRPC	0	When this bit is set to 1, it enables an interrupt when the Phase C reactive power (total or fundamental) identified by Bit 1 (REVRPSEL) in the MMODE register changes sign.
13	REVPSUM2	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF2 datapath changes sign.
14	CF1	0	When this bit is set to 1, it enables an interrupt when a high to low transition occurs at the CF1 pin; that is, an active low pulse is generated. The interrupt can be enabled even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL[2:0]) in the CFMODE register (see Table 52).
15	CF2	0	When this bit is set to 1, it enables an interrupt when a high to low transition occurs at the CF2 pin; that is, an active low pulse is generated. The interrupt can be enabled even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bits[5:3] (CF2SEL[2:0]) in the CFMODE register (see Table 52).
16	CF3	0	When this bit is set to 1, it enables an interrupt when a high to low transition occurs at the CF3 pin; that is, an active low pulse is generated. The interrupt can be enabled even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL[2:0]) in the CFMODE register (see Table 52).
17	DREADY	0	When this bit is set to 1, it enables an interrupt when all periodical (8 kHz rate) DSP computations finish.
18	REVPSUM3	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF3 datapath changes sign.
[31:19]	Reserved	0 0000 0000 0000	Reserved. These bits do not manage any functionality.

7.4.10 MASK1 Register (Address 0xE50B – Length 32 bits)

Table 48. MASK1 Register (Address 0xE50B)

Bits	Bit Name	Default Value	Description
0	NLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters the no load condition based on the total active and reactive powers.
1	FNLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters the no load condition based on the fundamental active and reactive powers.
2	VANLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters the no load condition based on the apparent power.
3	ZXTOVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on the Phase A voltage is missing.
4	ZXTOVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on the Phase B voltage is missing.
5	ZXTOVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on the Phase C voltage is missing.
6	ZXTOIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on the Phase A current is missing.
7	ZXTOIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on the Phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on the Phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on the Phase A voltage.
10	ZXVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on the Phase B voltage.
11	ZXVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on the Phase C voltage.
12	ZXIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on the Phase A current.
13	ZXIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on the Phase B current.
14	ZXIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on the Phase C current.
15	RSTDONE	0	Because the RSTDONE interrupt cannot be disabled, this bit has no function. It can be set to 1 or cleared to 0 with no effect on the device.
16	Sag	0	When this bit is set to 1, it enables an interrupt when a sag event occurs on the phase indicated by Bits[14:12] (VSPHASE[x]) in the PHSTATUS register (see Table 49).
17	OI	0	When this bit is set to 1, it enables an interrupt when an overcurrent event occurs on the phase indicated by Bits[5:3] (OIPHASE[x]) in the PHSTATUS register (see Table 49).
18	OV	0	When this bit is set to 1, it enables an interrupt when an overvoltage event occurs on the phase indicated by Bits[11:9] (OVPHASE[x]) in the PHSTATUS register (see Table 49).
19	SEQERR	0	When this bit is set to 1, it enables an interrupt when a negative to positive zero crossing on the Phase A voltage is followed by a negative to positive zero crossing on the Phase C voltage instead of on the Phase B voltage.
20	MISMTCH	0	When this bit is set to 1, it enables an interrupt when ||ISUM| – |INWV|| > |ISUMLVL|, where ISUMLVL is the value of the ISUMLVL register (Address 0x4398). For more information, see the Neutral Current Mismatch section.
[22:21]	Reserved	00	Reserved. These bits do not manage any functionality.
23	PKI	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the current channel has ended.
24	PKV	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the voltage channel has ended.
25	CRC	0	When this bit is set to 1, it enables an interrupt when the latest checksum value is different from the checksum value computed when the run register was set to 1.
[31:26]	Reserved	00 0000	Reserved. These bits do not manage any functionality.

7.4.11 PHSTATUS Register (Address 0xE600 – Length 16 bits)

Table 49. PHSTATUS Register (Address 0xE600)

Bits	Bit Name	Default Value	Description
[2:0]	Reserved	000	Reserved. These bits are always set to 0.
3	OIPHASE[0]	0	When this bit is set to 1, the Phase A current generates Bit 17 (OI) in the STATUS1 register.
4	OIPHASE[1]	0	When this bit is set to 1, the Phase B current generates Bit 17 (OI) in the STATUS1 register.
5	OIPHASE[2]	0	When this bit is set to 1, the Phase C current generates Bit 17 (OI) in the STATUS1 register.
[8:6]	Reserved	000	Reserved. These bits are always set to 0.
9	OVPHASE[0]	0	When this bit is set to 1, the Phase A voltage generates Bit 18 (OV) in the STATUS1 register.
10	OVPHASE[1]	0	When this bit is set to 1, the Phase B voltage generates Bit 18 (OV) in the STATUS1 register.
11	OVPHASE[2]	0	When this bit is set to 1, the Phase C voltage generates Bit 18 (OV) in the STATUS1 register.
12	VSPHASE[0]	0	When this bit is set to 1, the Phase A voltage generates Bit 16 (sag) in the STATUS1 register.
13	VSPHASE[1]	0	When this bit is set to 1, the Phase B voltage generates Bit 16 (sag) in the STATUS1 register.
14	VSPHASE[2]	0	When this bit is set to 1, the Phase C voltage generates Bit 16 (sag) in the STATUS1 register.
15	Reserved	0	Reserved. This bit is always set to 0.

7.4.12 PHNOLOAD Register (Address 0xE608 - – Length 16 bits)

Table 50. PHNOLOAD Register (Address 0xE608)

Bits	Bit Name	Default Value	Description
0	NLPHASE[0]	0	0: Phase A is out of the no load condition based on the total active and reactive powers. 1: Phase A is in the no load condition based on the total active and reactive powers. This bit is set together with Bit 0 (NLOAD) in the STATUS1 register.
1	NLPHASE[1]	0	0: Phase B is out of the no load condition based on the total active and reactive powers. 1: Phase B is in the no load condition based on the total active and reactive powers. This bit is set together with Bit 0 (NLOAD) in the STATUS1 register.
2	NLPHASE[2]	0	0: Phase C is out of the no load condition based on the total active and reactive powers. 1: Phase C is in the no load condition based on the total active and reactive powers. This bit is set together with Bit 0 (NLOAD) in the STATUS1 register.
3	FNLPHASE[0]	0	0: Phase A is out of the no load condition based on the fundamental active and reactive powers. 1: Phase A is in the no load condition based on the fundamental active and reactive powers. This bit is set together with Bit 1 (FNLOAD) in the STATUS1 register.
4	FNLPHASE[1]	0	0: Phase B is out of the no load condition based on the fundamental active and reactive powers. 1: Phase B is in the no load condition based on the fundamental active and reactive powers. This bit is set together with Bit 1 (FNLOAD) in the STATUS1 register.
5	FNLPHASE[2]	0	0: Phase C is out of the no load condition based on the fundamental active and reactive powers. 1: Phase C is in the no load condition based on the fundamental active and reactive powers. This bit is set together with Bit 1 (FNLOAD) in the STATUS1 register.
6	VANLPHASE[0]	0	0: Phase A is out of the no load condition based on the apparent power. 1: Phase A is in the no load condition based on the apparent power. This bit is set together with Bit 2 (VANLOAD) in the STATUS1 register.
7	VANLPHASE[1]	0	0: Phase B is out of the no load condition based on the apparent power. 1: Phase B is in the no load condition based on the apparent power. This bit is set together with Bit 2 (VANLOAD) in the STATUS1 register.
8	VANLPHASE[2]	0	0: Phase C is out of the no load condition based on the apparent power. 1: Phase C is in the no load condition based on the apparent power. This bit is set together with Bit 2 (VANLOAD) in the STATUS1 register.
[15:9]	Reserved	000 0000	Reserved. These bits are always set to 0.

7.4.13 COMPMODE Register (Address 0xE60E – Length 16 bits)

Table 51. COMPMODE Register (Address 0xE60E)

Bits	Bit Name	Default Value	Description
0	TERMSEL1[0]	1	0: Phase A is not included in the CF1 output calculations. 1: Phase A is included in the CF1 output calculations. Setting the TERMSEL1[2:0] bits to 111 specifies that the sum of all three phases is included in the CF1 output.
1	TERMSEL1[1]	1	0: Phase B is not included in the CF1 output calculations. 1: Phase B is included in the CF1 output calculations. Setting the TERMSEL1[2:0] bits to 111 specifies that the sum of all three phases is included in the CF1 output.
2	TERMSEL1[2]	1	0: Phase C is not included in the CF1 output calculations. 1: Phase C is included in the CF1 output calculations. Setting the TERMSEL1[2:0] bits to 111 specifies that the sum of all three phases is included in the CF1 output.
3	TERMSEL2[0]	1	0: Phase A is not included in the CF2 output calculations. 1: Phase A is included in the CF2 output calculations. Setting the TERMSEL2[2:0] bits to 111 specifies that the sum of all three phases is included in the CF2 output.
4	TERMSEL2[1]	1	0: Phase B is not included in the CF2 output calculations. 1: Phase B is included in the CF2 output calculations. Setting the TERMSEL2[2:0] bits to 111 specifies that the sum of all three phases is included in the CF2 output.
5	TERMSEL2[2]	1	0: Phase C is not included in the CF2 output calculations. 1: Phase C is included in the CF2 output calculations. Setting the TERMSEL2[2:0] bits to 111 specifies that the sum of all three phases is included in the CF2 output.
6	TERMSEL3[0]	1	0: Phase A is not included in the CF3 output calculations. 1: Phase A is included in the CF3 output calculations. Setting the TERMSEL3[2:0] bits to 111 specifies that the sum of all three phases is included in the CF3 output.
7	TERMSEL3[1]	1	0: Phase B is not included in the CF3 output calculations. 1: Phase B is included in the CF3 output calculations. Setting the TERMSEL3[2:0] bits to 111 specifies that the sum of all three phases is included in the CF3 output.
8	TERMSEL3[2]	1	0: Phase C is not included in the CF3 output calculations. 1: Phase C is included in the CF3 output calculations. Setting the TERMSEL3[2:0] bits to 111 specifies that the sum of all three phases is included in the CF3 output.
[10:9]	ANGLESEL[1:0]	00	00: delays between the voltages and currents of the same phase are measured. 01: delays between the phase voltages are measured. 10: delays between the phase currents are measured. 11: no delays are measured.
11	VNOMAEN	0	0: the apparent power on Phase A is computed normally by multiplying the voltage rms value by the current rms value. 1: the apparent power on Phase A is computed by multiplying the phase rms current by an rms voltage written to the VNOM register (Address 0xE533).
12	VNOMBEN	0	0: the apparent power on Phase B is computed normally by multiplying the voltage rms value by the current rms value. 1: the apparent power on Phase B is computed by multiplying the phase rms current by an rms voltage written to the VNOM register (Address 0xE533).
13	VNOMCEN	0	0: the apparent power on Phase C is computed normally by multiplying the voltage rms value by the current rms value. 1: the apparent power on Phase C is computed by multiplying the phase rms current by an rms voltage written to the VNOM register (Address 0xE533).
14	SELFREQ	0	0: ADE7978 is connected to a 50 Hz network. 1: ADE7978 is connected to a 60 Hz network.
15	Reserved	0	This bit is set to 0 by default and does not manage any functionality.

7.4.14 CFMODE Register (Address 0xE610 – Length 16 bits)

Table 52. CFMODE Register (Address 0xE610)

Bits	Bit Name	Default Value	Description
[2:0]	CF1SEL[2:0]	000	000: CF1 frequency is proportional to the sum of the total active powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 001: CF1 frequency is proportional to the sum of the total reactive powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 010: CF1 frequency is proportional to the sum of the apparent powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 011: CF1 frequency is proportional to the sum of the fundamental active powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 100: CF1 frequency is proportional to the sum of the fundamental reactive powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 101, 110, 111: reserved. The CF1 signal is not generated.
[5:3]	CF2SEL[2:0]	001	000: CF2 frequency is proportional to the sum of the total active powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 001: CF2 frequency is proportional to the sum of the total reactive powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 010: CF2 frequency is proportional to the sum of the apparent powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 011: CF2 frequency is proportional to the sum of the fundamental active powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 100: CF2 frequency is proportional to the sum of the fundamental reactive powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 101, 110, 111: reserved. The CF2 signal is not generated.
[8:6]	CF3SEL[2:0]	010	000: CF3 frequency is proportional to the sum of the total active powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 001: CF3 frequency is proportional to the sum of the total reactive powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 010: CF3 frequency is proportional to the sum of the apparent powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 011: CF3 frequency is proportional to the sum of the fundamental active powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 100: CF3 frequency is proportional to the sum of the fundamental reactive powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 101, 110, 111: reserved. The CF3 signal is not generated.
9	CF1DIS	1	0: CF1 output is enabled. 1: CF1 output is disabled. The energy-to-frequency converter remains enabled.
10	CF2DIS	1	0: CF2 output is enabled. 1: CF2 output is disabled. The energy-to-frequency converter remains enabled.
11	CF3DIS	1	0: CF3 output is enabled. 1: CF3 output is disabled. The energy-to-frequency converter remains enabled.
12	CF1LATCH	0	0: no latching of energy registers occurs when a CF1 pulse is generated. 1: the contents of the corresponding energy registers are latched when a CF1 pulse is generated. See the Synchronizing Energy Registers with the CFx Outputs section.
13	CF2LATCH	0	0: no latching of energy registers occurs when a CF2 pulse is generated. 1: the contents of the corresponding energy registers are latched when a CF2 pulse is generated. See the Synchronizing Energy Registers with the CFx Outputs section.
14	CF3LATCH	0	0: no latching of energy registers occurs when a CF3 pulse is generated. 1: the contents of the corresponding energy registers are latched when a CF3 pulse is generated. See the Synchronizing Energy Registers with the CFx Outputs section.
15	Reserved	0	Reserved. This bit does not manage any functionality.

7.4.15 APHCAL, BPHCAL, CPHCAL Registers (Address: 0xE614 – 0xE615 – 0xE616)

Table 53. APHCAL, BPHCAL, CPHCAL Registers (Address 0xE614, Address 0xE615, Address 0xE616)

Bits	Bit Name	Default Value	Description
[9:0]	PHCALVAL	0000000000	If current channel compensation is necessary, these bits can be set to a value from 0 to 383. If voltage channel compensation is necessary, these bits can be set to a value from 512 to 895. If the PHCALVAL bits are set to values from 384 to 511, the compensation behaves in the same way as when the PHCALVAL bits are set to values from 0 to 127. If the PHCALVAL bits are set to values from 896 to 1023, the compensation behaves in the same way as when the PHCALVAL bits are set to values from 512 and 639.
[15:10]	Reserved	000000	Reserved. These bits do not manage any functionality.

7.4.16 PHSIGN Register (Address 0xE617 – Length 16 bits)

Table 54. PHSIGN Register (Address 0xE617)

Bits	Bit Name	Default Value	Description
0	AWSIGN	0	0: the Phase A active power (total or fundamental, as specified by Bit 0 (REVAPSEL) in the MMODE register) is positive. 1: the Phase A active power (total or fundamental, as specified by Bit 0 (REVAPSEL) in the MMODE register) is negative.
1	BWSIGN	0	0: the Phase B active power (total or fundamental, as specified by Bit 0 (REVAPSEL) in the MMODE register) is positive. 1: the Phase B active power (total or fundamental, as specified by Bit 0 (REVAPSEL) in the MMODE register) is negative.
2	CWSIGN	0	0: the Phase C active power (total or fundamental, as specified by Bit 0 (REVAPSEL) in the MMODE register) is positive. 1: the Phase C active power (total or fundamental, as specified by Bit 0 (REVAPSEL) in the MMODE register) is negative.
3	SUM1SIGN	0	0: the sum of all phase powers in the CF1 datapath is positive. 1: the sum of all phase powers in the CF1 datapath is negative. Phase powers in the CF1 datapath are identified by Bits[2:0] (TERMSEL1[x]) of the COMPMODE register and by Bits[2:0] (CF1SEL[2:0]) of the CFMODE register.
4	AVARSIGN	0	0: the Phase A reactive power (total or fundamental, as specified by Bit 1 (REVRPSEL) in the MMODE register) is positive. 1: the Phase A reactive power (total or fundamental, as specified by Bit 1 (REVRPSEL) in the MMODE register) is negative.
5	BVARSIGN	0	0: the Phase B reactive power (total or fundamental, as specified by Bit 1 (REVRPSEL) in the MMODE register) is positive. 1: the Phase B reactive power (total or fundamental, as specified by Bit 1 (REVRPSEL) in the MMODE register) is negative.
6	CVARSIGN	0	0: the Phase C reactive power (total or fundamental, as specified by Bit 1 (REVRPSEL) in the MMODE register) is positive. 1: the Phase C reactive power (total or fundamental, as specified by Bit 1 (REVRPSEL) in the MMODE register) is negative.
7	SUM2SIGN	0	0: the sum of all phase powers in the CF2 datapath is positive. 1: the sum of all phase powers in the CF2 datapath is negative. Phase powers in the CF2 datapath are identified by Bits[5:3] (TERMSEL2[x]) of the COMPMODE register and by Bits[5:3] (CF2SEL[2:0]) of the CFMODE register.
8	SUM3SIGN	0	0: the sum of all phase powers in the CF3 datapath is positive. 1: the sum of all phase powers in the CF3 datapath is negative. Phase powers in the CF3 datapath are identified by Bits[8:6] (TERMSEL3[x]) of the COMPMODE register and by Bits[8:6] (CF3SEL[2:0]) of the CFMODE register.
[15:9]	Reserved	000 0000	Reserved. These bits are always set to 0.

7.4.17 CONFIG Register (Address 0xE618 – Length 16 bits)

Table 55. CONFIG Register (Address 0xE618)

Bits	Bit Name	Default Value	Description
[1:0]	ZX_DREADY	00	This bit manages the output signal at the ZX/$\overline{\text{DREADY}}$ pin. For more information about the zero-crossing function, see the Zero-Crossing Detection section. 00: $\overline{\text{DREADY}}$ functionality is enabled (see the Digital Signal Processor section). 01: ZX functionality is generated by the Phase A voltage. 10: ZX functionality is generated by the Phase B voltage. 11: ZX functionality is generated by the Phase C voltage.
2	Reserved	0	Reserved. This bit is always set to 0.
3	Swap	0	1: the voltage channel outputs VA, VB, VC, and VN are swapped with the current channel outputs IA, IB, IC, and IN, respectively. Thus, the current channel information is present in the phase voltage channel registers and vice versa.
4	HPFEN	1	0: all high-pass filters in the voltage and current channels are disabled. 1: all high-pass filters in the voltage and current channels are enabled.
5	LPFSEL	0	This bit specifies the settling time introduced by the low-pass filter in the total active power datapath. 0: settling time = 650 ms. 1: settling time = 1300 ms.
6	HSDCEN	0	0: HSDC serial port is disabled and CF3 functionality is configured on the CF3/HSCLK pin. 1: HSDC serial port is enabled and HSCLK functionality is configured on the CF3/HSCLK pin.
7	SWRST	0	When this bit is set to 1, a software reset is initiated.
[9:8]	VTOIA[1:0]	00	These bits select the phase voltage that is considered together with the Phase A current in the power path. 00: Phase A voltage. 01: Phase B voltage. 10: Phase C voltage. 11: reserved (same as VTOIA[1:0] = 00).
[11:10]	VTOIB[1:0]	00	These bits select the phase voltage that is considered together with the Phase B current in the power path. 00: Phase B voltage. 01: Phase C voltage. 10: Phase A voltage. 11: reserved (same as VTOIB[1:0] = 00).
[13:12]	VTOIC[1:0]	00	These bits select the phase voltage that is considered together with the Phase C current in the power path. 00: Phase C voltage. 01: Phase A voltage. 10: Phase B voltage. 11: reserved (same as VTOIC[1:0] = 00).
14	INSEL	0	0: the NIRMS register (Address 0x43C9) contains the rms value of the neutral current. 1: the NIRMS register contains the rms value of ISUM, the instantaneous value of the sum of all three phase currents, IA, IB, and IC.
15	Reserved	0	Reserved. This bit does not manage any functionality.

7.4.18 MMODE Register (Address 0xE700 – Length 8 bits)

Table 56. MMODE Register (Address 0xE700)

Bits	Bit Name	Default Value	Description
0	REVAPSEL	0	This bit specifies whether the total active power or the fundamental active power on Phase A, Phase B, or Phase C is used to trigger a bit in the STATUS0 register. Phase A triggers Bit 6 (REVAPA), Phase B triggers Bit 7 (REVAPB), and Phase C triggers Bit 8 (REVAPC). 0: The total active power is used to trigger the bits in the STATUS0 register. 1: The fundamental active power is used to trigger the bits in the STATUS0 register.
1	REVRPSEL	0	This bit specifies whether the total reactive power or the fundamental reactive power on Phase A, Phase B, or Phase C is used to trigger a bit in the STATUS0 register. Phase A triggers Bit 10 (REVRPA), Phase B triggers Bit 11 (REVRPB), and Phase C triggers Bit 12 (REVRPC). 0: The total reactive power is used to trigger the bits in the STATUS0 register. 1: The fundamental reactive power is used to trigger the bits in the STATUS0 register.
2	PEAKSEL[0]	1	0: Phase A is not included in the voltage and current peak detection. 1: Phase A is included in the voltage and current peak detection.
3	PEAKSEL[1]	1	0: Phase B is not included in the voltage and current peak detection. 1: Phase B is included in the voltage and current peak detection.
4	PEAKSEL[2]	1	0: Phase C is not included in the voltage and current peak detection. 1: Phase C is included in the voltage and current peak detection.
[7:5]	Reserved	000	Reserved. These bits do not manage any functionality.

7.4.19 ACCMODE Register (Address 0xE701 – Length 8 bits)

Table 57. ACCMODE Register (Address 0xE701)

Bits	Bit Name	Default Value	Description
[1:0]	WATTACC[1:0]	00	These bits determine how the active power is accumulated in the watthour registers and how the CFx frequency output is generated as a function of the total and fundamental active powers. 00: signed accumulation mode of the total and fundamental active powers. The active energy registers and the CFx pulses are generated in the same way. 01: positive only accumulation mode of the total and fundamental active powers. The total and fundamental active energy registers are accumulated in positive only mode, but the CFx pulses are generated in signed accumulation mode. 10: reserved (same as WATTACC[1:0] = 00). 11: absolute accumulation mode of the total and fundamental active powers. The total and fundamental active energy registers and the CFx pulses are generated in the same way.
[3:2]	VARACC[1:0]	00	These bits determine how the reactive power is accumulated in the var-hour registers and how the CFx frequency output is generated as a function of the total and fundamental active and reactive powers. 00: signed accumulation mode of the total and fundamental reactive powers. The reactive energy registers and the CFx pulses are generated in the same way. 01: reserved (same as VARACC[1:0] = 00). 10: the total and fundamental reactive powers are accumulated depending on the sign of the total and fundamental active powers. If the active power is positive, the reactive power is accumulated as is; if the active power is negative, the reactive power is accumulated with a reversed sign. The total and fundamental reactive energy registers and the CFx pulses are generated in the same way. 11: absolute accumulation mode of the total and fundamental reactive powers. The total and fundamental reactive energy registers and the CFx pulses are generated in the same way.
[5:4]	CONSEL[1:0]	00	These bits select the inputs to the energy accumulation registers. IA', IB', and IC' are IA, IB, and IC shifted by –90° (see Table 58). 00: 3-phase, 4-wire with three voltage sensors. 01: 3-phase, 3-wire delta connection. 10: reserved. 11: 3-phase, 4-wire delta connection.
6	SAGCFG	0	This bit manages how the sag flag status bit in the STATUS1 register is generated. 0: the flag is set to 1 when any phase voltage is below the SAGLVL threshold. 1: the flag is set to 1 when any phase voltage goes below and then above the SAGLVL threshold.
7	Reserved	1	Reserved. This bit does not manage any functionality.

7.4.20 CONSEL[1:0] Bits in Energy Registers

Table 58. CONSEL[1:0] Bits in Energy Registers[1]

Energy Registers	CONSEL[1:0] = 00	CONSEL[1:0] = 01	CONSEL[1:0] = 11
AWATTHR, AFWATTHR	VA × IA	VA × IA	VA × IA
BWATTHR, BFWATTHR	VB × IB	VB = VA – VC	VB = –VA
		VB × IB[1]	VB × IB
CWATTHR, CFWATTHR	VC × IC	VC × IC	VC × IC
AVARHR, AFVARHR	VA × IA′	VA × IA′	VA × IA′
BVARHR, BFVARHR	VB × IB′	VB = VA – VC	VB = –VA
		VB × IB′[1]	VB × IB′
CVARHR, CFVARHR	VC × IC′	VC × IC′	VC × IC′
AVAHR	VA rms × IA rms	VA rms × IA rms	VA rms × IA rms
BVAHR	VB rms × IB rms	VB rms × IB rms[1]	VB rms × IB rms
		VB = VA – VC	VB = –VA
CVAHR	VC rms × IC rms	VC rms × IC rms	VC rms × IC rms

[1] In a 3-phase, 3-wire configuration (CONSEL[1:0] = 01), the ADE7978 computes the rms value of the line voltage between Phase A and Phase C and stores the result in the BVRMS register (see the Voltage RMS in Delta Configurations section). The Phase B current value provided after the HPF is 0. Consequently, the powers associated with Phase B are 0. To avoid any errors in the frequency output pins (CF1, CF2, or CF3) related to the powers associated with Phase B, disable the contribution of Phase B to the energy-to-frequency converters by setting the TERMSEL1[1], TERMSEL2[1], or TERMSEL3[1] bit to 0 in the COMPMODE register. For more information, see the Energy-to-Frequency Conversion section.

7.4.21 LCYCMODE Register (Address 0xE702 – Length 8 bits)

Table 59. LCYCMODE Register (Address 0xE702)

Bits	Bit Name	Default Value	Description
0	LWATT	0	0: the watthour accumulation registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) are configured for regular accumulation mode. 1: the watthour accumulation registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) are configured for line cycle accumulation mode.
1	LVAR	0	0: the var-hour accumulation registers (AVARHR, BVARHR, CVARHR, AFVARHR, BFVARHR, and CFVARHR) are configured for regular accumulation mode. 1: the var-hour accumulation registers (AVARHR, BVARHR, CVARHR, AFVARHR, BFVARHR, and CFVARHR) are configured for line cycle accumulation mode.
2	LVA	0	0: the VA-hour accumulation registers (AVAHR, BVAHR, and CVAHR) are configured for regular accumulation mode. 1: the VA-hour accumulation registers (AVAHR, BVAHR, and CVAHR) are configured for line cycle accumulation mode.
3	ZXSEL[0]	1	0: Phase A is not selected for zero-crossing counts in line cycle accumulation mode. 1: Phase A is selected for zero-crossing counts in line cycle accumulation mode. If more than one phase is selected for zero-crossing detection, the accumulation time is shortened accordingly.
4	ZXSEL[1]	1	0: Phase B is not selected for zero-crossing counts in line cycle accumulation mode. 1: Phase B is selected for zero-crossing counts in line cycle accumulation mode. If more than one phase is selected for zero-crossing detection, the accumulation time is shortened accordingly.
5	ZXSEL[2]	1	0: Phase C is not selected for zero-crossing counts in line cycle accumulation mode. 1: Phase C is selected for zero-crossing counts in line cycle accumulation mode. If more than one phase is selected for zero-crossing detection, the accumulation time is shortened accordingly.
6	RSTREAD	1	0: disables read with reset of all xWATTHR, xVARHR, xVAHR, xFWATTHR, and xFVARHR registers. Clear this bit to 0 when Bits[2:0] (LVA, LVAR, and LWATT) are set to 1. 1: enables read with reset of all xWATTHR, xVARHR, xVAHR, xFWATTHR, and xFVARHR registers. When this bit is set to 1, a read of these registers resets them to 0.
7	PFMODE	0	0: power factor calculation uses instantaneous values of various phase powers used in its expression. 1: power factor calculation uses phase energy values calculated using line cycle accumulation mode. The LWATT and LVA bits (Bit 0 and Bit 2) must be enabled for the power factors to be computed correctly. The update rate of the power factor measurement is the integral number of half line cycles that is programmed in the LINECYC register.

7.4.22 HSDC_CFG Register (Address 0xE706 – Length 8 bits)

Table 60. HSDC_CFG Register (Address 0xE706)

Bits	Bit Name	Default Value	Description
0	HCLK	0	0: HSCLK is 8 MHz. 1: HSCLK is 4 MHz.
1	HSIZE	0	0: HSDC transmits the 32-bit registers in 32-bit packages, most significant bit first. 1: HSDC transmits the 32-bit registers in 8-bit packages, most significant bit first.
2	HGAP	0	0: no gap is introduced between packages. 1: a gap of seven HCLK cycles is introduced between packages.
[4:3]	HXFER[1:0]	00	00: HSDC transmits sixteen 32-bit words in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, INWV, AVA, BVA, CVA, AWATT, BWATT, CWATT, AVAR, BVAR, and CVAR. 01: HSDC transmits seven instantaneous values of currents and voltages in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, and INWV. 10: HSDC transmits nine instantaneous values of phase powers in the following order: AVA, BVA, CVA, AWATT, BWATT, CWATT, AVAR, BVAR, and CVAR. 11: reserved (same as HXFER[1:0] = 00).
5	HSAPOL	0	0: $\overline{SS}$/HSA output pin is active low. 1: $\overline{SS}$/HSA output pin is active high.
[7:6]	Reserved	00	Reserved. These bits do not manage any functionality.

7.4.23 CONFIG3 Register (Address 0xE708 – Length 8 bits)

Table 61. CONFIG3 Register (Address 0xE708)

Bits	Bit Name	Default Value	Description
0	VA2_EN	1	This bit configures the V2 channel or temperature measurement on the Phase A ADE7933/ADE7932. 0: temperature sensor is measured on the second voltage channel of the Phase A ADE7933/ADE7932. On the ADE7932, the temperature sensor is always sensed by the second voltage channel, but this bit must still be cleared to 0 to enable the temperature measurement. 1: V2P input is sensed on the second voltage channel of the Phase A ADE7933.
1	VB2_EN	1	This bit configures the V2 channel or temperature measurement on the Phase B ADE7933/ADE7932. 0: temperature sensor is measured on the second voltage channel of the Phase B ADE7933/ADE7932. On the ADE7932, the temperature sensor is always sensed by the second voltage channel, but this bit must still be cleared to 0 to enable the temperature measurement. 1: V2P input is sensed on the second voltage channel of the Phase B ADE7933.
2	VC2_EN	1	This bit configures the V2 channel or temperature measurement on the Phase C ADE7933/ADE7932. 0: temperature sensor is measured on the second voltage channel of the Phase C ADE7933/ADE7932. On the ADE7932, the temperature sensor is always sensed by the second voltage channel, but this bit must still be cleared to 0 to enable the temperature measurement. 1: V2P input is sensed on the second voltage channel of the Phase C ADE7933.
3	VN2_EN	1	This bit configures the V2 channel or temperature measurement on the neutral line ADE7923 or ADE7933/ADE7932. 0: temperature sensor is measured on the second voltage channel of the neutral line ADE7933/ ADE7932 and ADE7923. On the ADE7932, the temperature sensor is always sensed by the second voltage channel, but this bit must still be cleared to 0 to enable the temperature measurement. 1: V2P input is sensed on the second voltage channel of the neutral line ADE7933 and ADE7923.
[5:4]	Reserved	00	Reserved. These bits do not manage any functionality.
6	CLKOUT_DIS	0	0: ADE7933/ADE7932 and ADE7923 CLKOUT pins are enabled. 1: ADE7933/ADE7932 and ADE7923 CLKOUT pins are set high and no clock is generated.
7	ADE7933_ SWRST	0	When this bit is set to 1, a software reset of the ADE7933/ADE7932 and ADE7923 devices is initiated. See the ADE7933/ADE7932 and ADE7923 Software Reset section for more information.

7.4.24 CONFIG2 Register (Address 0xEA00 – Length 8 bits)

Table 62. CONFIG2 Register (Address 0xEA00)

Bits	Bit Name	Default Value	Description
0	I2C_LOCK	0	When this bit is set to 0, the $\overline{SS}$/HSA pin can be toggled three times to activate the SPI serial port. If I^2C is the selected serial port, set this bit to 1 to lock the selection. After a 1 is written to this bit, the ADE7978 ignores spurious toggling of the $\overline{SS}$/HSA pin. If SPI is the selected serial port, any write to the CONFIG2 register locks the selection. The communication protocol can be changed only after a power-down or hardware reset operation.
[7:1]	Reserved	000 0000	Reserved. These bits do not manage any functionality.